

ICS 31.200
CCS L 56

SJ

**INDUSTRY STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

SJ/Z 11360-2006

Integrated circuit IP core signal integrity specification

集成电路IP核信号完整性规范

(English Translation)

Issued on: September 26, 2006

Implemented on: December 1, 2006

Issued by: Ministry of Industry and Information Technology

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What this standard covers

This standard specifies the SoC design digital and analog/mixed-signal IP cores (IntellectualPropertyCore, hereinafter referred to as IP) and signal integrity (SI) problems related deliverables, data formats, and related design criteria and design examples are given. This specification focuses on the SoC design process, IP designers and IP integrators for digital and analog/mixed-signal integrated module requires both communicating SI issues, including interface design. IP in this specification refers to the hard blocks are provided in the form. This specification is limited to the power supply grid, and Crosstalk uniformly doped silicon substrate and the heavily doped bulk silicon substrate, a silicon substrate, an epitaxial layer of substrate coupling. This specification also relates to the power grid, and migration problems associated signal. This specification does not involve noise SI IC packaging problem. This specification focuses on 0.18μm technology generations, but also related to 0.07μm and below process may occur in the SI issue. Although SI above question is based on 0.18μm technology experience, but most of its content can be used to help the IP in the transfer of these processes. However, this specification focuses on meeting the most IP designers and integrators design requirements of the specific process node scope.

Document data

International classification (ICS): 31.200.

Chinese classification (CCS): L56.

Estimated length of the Chinese original: 46,416 words.

Standards quoted by this document

SJ/Z 11354-2006; SJ/Z 11357-2006