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JJG

**INDUSTRY STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

JJG 957-2015

Replacing JJG 957-2000

**Verification Regulation of Logic Analyzers
(English Translation)**

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Introduction

This procedure is JJG 957-2000 "logic analyzer test procedures" amendments. Procedures based JJF1002-2010 "National verification procedures to write the rules," revised. The main technical changes are as follows.

- The original statutes timing analysis and state analysis speed clock rate has been extended, were the original 100MHz Up to 5GHz and 50MHz up to 2GHz;
- The original statutes minimum clock pulse width is extended, the original 5ns to 200ps;
- Setup and data in the original protocol data retention time is measured has been revised, the original 0ns ~ 50ns to setup/hold time window measuring range of 180ps ~ 10ns;
- The original regulations can be detected in the narrowest width of the glitch has been revised, the original 0.5ns to 1ns;
- The original statutes threshold level measurement range has been revised to former -20V ~ 20V-10V ~ 10V;
- The original statutes verification project was amended to remove the highest clock mixed mode operation state analysis Clock rate test, the new increase minimum pulse width (200ps) and time intervals (≥ 1 ns) verification.

The regulations previously issued as follows.

--- JJG 957-2000.

Logic analyzer test procedures

1 Scope

The order applies to the logic analyzer's initial verification, use and subsequent verification check.

2 Overview

Logic analyzer is mainly used for debugging hardware and software of a digital circuit having a plurality of data channels and a plurality of synchronous clock Characteristics that can facilitate the analysis of digital logic circuits. Divided into logical signals from the principle of timing analysis and logic State analysis of the signal by the multiplexer logic probe input data signal to logic "1" to "0" data status display. can Multi-stage trigger to collect data, you can display a list of the status of data collection mode or wave mode.

3 metering performance requirements

3.1 Timing Analysis

- a) threshold level. -10V ~ 10V, the maximum permissible error. $\pm (1\% \times \text{reading } 35\text{mV})$;
- b) minimum pulse width. 200ps (maximum clock speed 5GHz);
- c) glitch detection width. 1ns;
- d) Time interval measurement. ≥ 1 ns, the maximum permissible error. $\pm (0.01\% \times \text{reading a sampling period})$.

3.2 Status Analysis

- a) state the maximum clock speed. 2GHz;
- b) state the minimum clock pulse width. 200ps;
- c) the data setup/hold time window (Tw). 180ps ~ 10ns.

4 General technical requirements

4.1 Exterior Accessories Logic analyzer should look good, no effect on normal work of mechanical damage. Power supply clear signs, and set Set correctly. Accessories and operating instructions should be complete.

4.2 The normal sex

After energizing the logic analyzer screen should be normal, all the switches, buttons and knobs should be solid and reliable installation, location Accurate, good contact, smooth adjustment after the Power On Self Test by various indicators show should be normal.

5 control of measuring instruments

5.1.1 Environmental conditions Verification

- a) Ambient temperature. $23\text{ }^{\circ}\text{C} \pm 5\text{ }^{\circ}\text{C}$;
- b) Relative humidity. $\leq 80\%$;
- c) Power supply. $220\text{V} \pm 11\text{V}$, $50\text{Hz} \pm 1\text{Hz}$;