ICS 31.200
CCS L 55

NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/Z 43510-2023

Integrated circuit TSV 3D package reliability test methods guideline

集成电路TSV三维封装可靠性试验方法指南

Issued on: December 28, 2023 **Implemented on: April 1, 2024**

Issued by: State Administration for Market Regulation;
Standardization Administration of China

Table of Contents

1 Scope

2 Normative reference documents

3 Terms and definitions

Foreword

This document complies with the provisions of GB/T 1:1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents" Drafting: Please note that some content in this document may be subject to patents: The publisher of this document assumes no responsibility for identifying patents: This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China: This document is under the jurisdiction of the National Semiconductor Device Standardization Technical Committee (SAC/TC78): This document was drafted by: China Electronics Technology Standardization Institute, University of Electronic Science and Technology of China, Huajin Semiconductor Packaging Leading Technology R&D Center Co:, Ltd:, the 771st Research Institute of the Ninth Research Institute of China Aerospace Science and Technology Corporation, the Fifth Research Institute of Electronics of the Ministry of Industry and Information Technology, China Institute of Microelectronics, Academy of Sciences, Institute of Semiconductor, Chinese Academy of Sciences: The main drafters of this document: Li Kun, Peng Bo, Xiao Kelati, Wu Daowei, Zhou Bin, Gao Jiantou, and Li Wenchang: Integrated circuit TSV three-dimensional packaging reliability Test Method Guide

1 Scope

This document gives guidance on the reliability test methods for three-dimensional integrated circuit packages built with through-silicon vias, and applies to process verification for the three TSV manufacturing routes: via-first, via-middle and via-last. TSV is how a stack of dies is turned into one device, and it is where 3D packaging fails: a via that opens under thermal cycling, a copper pillar that voids, a stack that delaminates. The reliability question is not whether the package works when it leaves the line but whether it survives the field, and that can only be answered by tests that everyone runs the same way. Issued on 28 December 2023 by SAMR and SAC as a guiding technical document, in force from 1 April 2024, under the technical jurisdiction of the Ministry of Industry and Information Technology. Relevant to anyone qualifying an advanced package from a Chinese OSAT.

This document provides guidance on reliability test methods for process development and

verification of through silicon via (TSV) three-dimensional packaging: This document is applicable to the process verification of TSV three-dimensional packaging manufactured using three process processes: through-hole first, middle through-hole and through-last: test:

2 Normative reference documents

The contents of the following documents constitute essential provisions of this document through normative references in the text: Among them, the dated quotations For undated referenced documents, only the version corresponding to that date applies to this document; for undated referenced documents, the latest version (including all amendments) applies to this document: GB/T 4937:

4 Mechanical and climatic test methods for semiconductor devices Part 4: Highly accelerated steady-state hot and humid test (HAST) GB/T 4937:

11 Mechanical and climatic test methods for semiconductor devices Part 11: Rapid temperature change double liquid bath method GB/T 4937:

20 Mechanical and climatic test methods for semiconductor devices - Part 20: Resistance of plastic-encapsulated surface-mounted devices to moisture and soldering Comprehensive impact of heating GB/T 4937:

23 Mechanical and climatic test methods for semiconductor devices Part 23: High temperature operating life GB/T 4937:

30 Mechanical and climatic test methods for semiconductor devices Part 30: Reliability of non-sealed surface-mounted devices Pretreatment before test GB/T 4937:

42 Mechanical and climatic test methods for semiconductor devices Part 42: Temperature and humidity storage

GB/T 12750 Semiconductor device integrated circuits Part 11: Specifications for semiconductor integrated circuits (excluding hybrid circuits) IEC 60749-

5 Mechanical and climatic test methods for semiconductor devices Part 5: Steady-state temperature and humidity bias life test (Semi- biaslifetest) IEC 60749-

24 Mechanical and climatic test methods for semiconductor devices Part 24: Unbiased strongly accelerated steady-state damp heat test ance-UnbiasedHAST) IEC 60749-

29 Mechanical and climatic test methods for semiconductor devices Part 29: Latch-up test (Semiconductor

IEC 62374 Time-dependent (electrical) dielectric breakdown (TDDB) test of gate dielectric layer of semiconductor devices [Semiconductorde- grationtest)

3 Terms and definitions

The following terms and definitions apply to this document: