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**Photovoltaic modules - Test methods for the detection of
potential-induced degradation - Part 1-1: Crystalline silicon -
Delamination**

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(English Translation)

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Foreword

This document is a standard or guiding technical document.

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents".

Drafting.

This document is Part 1-1 of GB /Z 117 "Test Method for Potential-Induced Degradation of Photovoltaic Modules". GB /Z 117 has been published as follows.

Part 2.

---Part 1-1.Layering of Crystalline Silicon Modules This document is equivalent to IEC TS62804-1-1:2020 "Photovoltaic modules - Potential-induced degradation test methods - Part 1-1.Crystalline materials" The document type of "Layered Silicon Modules" has been changed from an IEC technical specification to a national standardization guidance technical document in my country.

Introduction

Potential-induced degradation (PID) refers to any photovoltaic degradation caused by potential stress between the cell circuitry and the outer surface or components of the photovoltaic module.

Module performance degradation. Moisture and system voltage factors may cause stratification (PID-d), which can lead to photovoltaic module stratification.

Problems such as electric shock, grounding faults, rapid moisture intrusion, and condensation buildup, along with corrosion and reduced photocurrent due to decreased battery light transmission performance, are also present.

It is associated with hot spot phenomenon and poor appearance.

GB /Z 117 "Test Method for Potential-Induced Degradation of Photovoltaic Modules" is proposed to consist of the following parts.

---Part 1: Crystalline Silicon Modules. Defines a test method for evaluating the power loss of crystalline silicon photovoltaic modules using PID (Potential Inversion and Degradation).

---Part 1-1: Crystalline Silicon Module Layering. Defines a test method for evaluating the layering of crystalline silicon photovoltaic modules using PID (Polymerization and Degradation).

---Part 2: Thin-film modules. Defines a test method for evaluating the power loss of thin-film photovoltaic modules using PID (Power Loss Assessment).

This document is used to test and evaluate the durability of crystalline silicon photovoltaic modules in stratification failure modes.

Studies have shown that the layering of crystalline silicon photovoltaic modules is related to the electrochemical reactions and metallization on the surface of crystalline silicon cells (Mon and Ross, (1985; Matsuda et al., 2012). Humidity can sometimes accelerate the decrease in interfacial adhesion of photovoltaic modules, accompanied by an increase in sodium ion concentration on the cell surface.

The increase in voltage may be a result of system voltage stress (Dhere et al., 2002; Bosco et al., 2017; Wohlgemuth et al., 2017; Li et al., 2018). Components using low volume resistivity encapsulation materials exhibit greater delamination under the electric field induced by system voltage.

Sensitivity (Hacke et al., 2016). Some components did not show a significant power loss due to PID shunting (PID-s) or PID polarization (PID-p) modes.

Attenuation, using the methods described in this document, may result in stratified degradation, such as when a battery, due to its tolerance to PID-s and PID-p, does not

exhibit power degradation.

Components with low resistivity but low volume resistivity due to reduced efficiency.

Studies have shown that for many encapsulants, increasing the dissolved water content increases their conductivity (Berghold et al., 2014). Therefore, This document provides an accelerated testing method to evaluate a component's sensitivity to stratification under conditions such as humidity and system voltage. While optimizing...

Installation and grounding configurations may mitigate PID failure modes, but as a test of laminates, the grounding of the glass surface and the assembly are discussed in this document.

It is unrelated to the expected installation and grounding configuration.

Under the influence of voltage potential, the conductivity of glass and the resulting charge transfer cause electrochemical reactions within the laminate. Therefore, this paper...

This mainly targets single-glass or double-glass modules. To date, measurements show that the volume resistivity of the module encapsulation differs by several orders of magnitude.

Therefore, based on the influence of volume resistivity on this stratification mode, this test scheme can distinguish between sensitive components and resistant components (Hacke et al.).

(Person, 2016). The test conditions in this document are highly accelerated and designed to differentiate components sensitive to stratified failure modes; however, they are suitable for various natural environments.

The acceleration factor for failure rate in the environment has not yet been determined. Appendix A illustrates the decay modes that occur after applying this method, as well as its practical applications.

Examples that are similar in appearance.

Layering may also occur through other mechanisms, such as photocatalytic reaction products (Matsuda et al., 2012), as described in this document or other existing literature.

This may not be reflected under standard testing methods.

It is well known that variations in manufacturing processes can affect the sensitivity of modules to voltage stress. Periodic retesting of module samples is necessary.

Including the above testing methods, it also includes internal quality assurance procedures (such as those specified in IEC TS62941) and external testing and verification, which helps to verify...

Verifying the impact of design on the voltage stress durability of components also helps to verify the effects of changes in materials and manufacturing processes.

Photovoltaic module potential-induced degradation test method Part 1-1. Layering of Crystalline Silicon Modules

1 Scope

This document describes the delamination (PID-d) failure phenomenon caused by partial potential-induced degradation in the laminates of single-glass or double-glass crystalline silicon photovoltaic modules.

This document describes test and evaluation methods for assessing stratification caused by current transfer between grounding and component battery circuits.

Factors contributing to accelerated stratification include damp heat exposure, sodium accumulation at the interface, cathode gas evolution in the battery circuit, metallization, and...

The decrease in adhesion of other components in the module due to voltage stimulation does not include power variations in the crystalline silicon photovoltaic module caused by stress factors.

The content falls within the scope of IEC TS62804-1.

The test method specified in this document involves testing the components in a humid and hot environment chamber, and applying the parameters specified in the component instruction manual to both electrodes of the components.

Or the maximum permissible system voltage. The actual durability of a component to system voltage stress depends on the installation design and the environmental conditions under which the component operates.

This test method evaluates the lamination of photovoltaic modules without considering the actual stress experienced by the modules during operation under different climatic and system conditions.

The sensitivity of the component to PID-d.

This document does not apply to different engineering methods for suppressing PID that may provide varying degrees of electrical isolation to the component surface.

Impacts include, for example, the use of rear rail brackets for installation, edge clamps for installation, and insulated frames.

2 Normative references

The contents of the following documents, through normative references within the text, constitute essential provisions of this document. Dated citations are not included.

For references to documents, only the version corresponding to that date applies to this