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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

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**Dynamic on-resistance test method guidelines for Gallium
Nitride High Electron Mobility Transistor (GaN HEMT) based
power conversion devices**

(English Translation)

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Table of Contents

Preface
Introduction
1 Scope
2 Normative References
3 Terms, Definitions, Symbols, and Abbreviations
3.1 Terms and Definitions
3.2 Symbols and Abbreviations
4 Test Circuit and Waveforms
4.1 General Provisions
4.3 Pulse Current-Voltage (IV) Method
5 Test Requirements 6.
References

Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents".

Drafting.

This document is equivalent to IEC 63373:2022 "Dynamic on-resistance of power conversion devices based on gallium nitride high electron mobility transistors".

Test Methodology Guide.

The following minimal editorial changes have been made to this document.

---The standard title has been changed to "Measurement of Dynamic On-Resistance of Gallium Nitride High Electron Mobility Transistors (GaNHEMTs) for Power Conversion".

Trial Methods Guide;

---The URLs for the ISO and IEC terminology databases have been removed;

---Corrected the symbol "VDS(ON)" in Figure 4 of section 4.2 to "VGS(OFF)".

Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents.

This document was proposed by the Ministry of Industry and Information Technology of the

People's Republic of China.

This document is under the jurisdiction of the National Semiconductor Device Standardization Technical Committee (SAC/TC78).

Introduction

This document provides a methodological guide for measuring the dynamic on-resistance of gallium nitride (GaN) power semiconductor devices, applicable to GaN power semiconductors.

The body and related power electronics industry.

Lateral GaN power high electron mobility transistors (HEMTs) are implemented through a two-dimensional electron gas (2DEG) channel in the on-state.

Current conduction occurs when devices are subjected to varying stresses in power electronic switching applications, which may cause some charge to be trapped in specific areas of the transistor.

Electrons are trapped in a loop. When a device operates in a switching state, the trapped electrons cause an increase in on-resistance; this phenomenon is called electrostatic discharge (ESD).

Current collapse. To distinguish it from DC on-resistance, the on-resistance of a switch during operation is also called dynamic on-resistance.

Increasing this will lead to higher power loss, thereby reducing the overall system efficiency. If the dynamic on-resistance characteristics are not verified, it will affect GaN...

Power devices face reliability risks.

The test methods provided in this document can serve as a guide for measuring the dynamic on-resistance of GaN power devices, with a focus on lateral GaN.

HEMT devices. The three test methods provided in this document can be used for product datasheets, process control, technology development, and final testing.

Applications. Parasitic effects can affect high-precision test results, while wafer-level testing can minimize these effects. Furthermore, self-heating effects may also affect the impact on package-level test results depends on the specific thermal characteristics of the package.

Gallium nitride high electron mobility transistors for power conversion

1 Scope

This document provides a methodological guide for testing the dynamic on-resistance of lateral GaNHEMTs. Dynamic on-resistance testing is primarily used for evaluation...

This test method can be applied to the following situations to estimate charge trapping phenomena in GaNHEMT.

- a) GaN enhancement-mode and depletion-mode discrete power devices;
- b) GaN integrated power chip;
- c) Wafer-level or package-level samples of the above objects.

The provided testing methods can be used for device characterization, product testing, reliability assessment, and application scenario verification in GaN power converters.

The document does not cover the basic principles of dynamic on-resistance or its symbolic representation in product specifications.

2 Normative references

This document has no normative references.

3.1 Terms and Definitions

This document does not contain any terms or definitions that need to be defined.

3.2 Symbols and Abbreviations

The following symbols and abbreviations apply to this document.

C. Capacitor.

DUT. Device Under Test.

D1. Freewheeling diode.

EPulse. Energy dissipated in a single pulse; applicable only to hard switches.

ID. Drain current in the DUT on state.

L. Inductance.

N. Number of pulses.

PPeak. Instantaneous peak power, applicable only to hard switching.

rDS(ON). Drain-source on-resistance in the DUT's on-state.

Rload. Load resistance.

TC. Shell temperature.

tdn. Soft switching delay time between the off-state and on-state pulses, n=1 or 2.

tm,on. Measurement delay of on-resistance during the on-state pulse.

toff. Pulse width in the off state.