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Micro-electromechanical systems (MEMS) technology - Requirements for the reliability evaluation of three-dimensional through-silicon via structures

微机电系统（MEMS）技术 硅通孔三维结构可靠性评价要求

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Foreword

The sample condition for TSV three-dimensional structural evaluation should be selected according to the following requirements.

a) Wafers are used for parameter evaluation;

b) Internal and external morphology evaluation uses wafers or chips, with chip-based evaluation used for sample preparation and microscopic examination;

c) Thermal stress characteristic evaluation uses wafers or chips, with steady-state lifetime and steady-state damp heat evaluation using chips;

d) Selection of chips for evaluating electrical stress characteristics;

e) Mechanical property evaluation uses chips fixed on a carrier;

f) Evaluation of interconnect characteristics and selection of chips;

g) Standard samples or chips are used for three-dimensional structural evaluation.

2 Block diagram of S-parameter testing system

6.1.3.2 Reporting Requirements The report should include at least the following.

a) Name and address of the manufacturing unit, product name, batch number, etc.;

b) Test environment. temperature, humidity, cleanliness, etc.;

c) Test equipment. model, name, and serial number;

d) Test temperature;

e) Sample quantity and distribution;

f) Test methods, criteria, test procedures and results, and test duration;

g) S-parameter values;

h) Failure analysis report (if any).

5 Failure Modes and Reliability Evaluation

5.1 Failure Mode Classification The failure modes of TSV three-dimensional structures are classified as follows:

a) Common failure modes in parameter evaluation include. 1) Increased DC resistance caused by defects in the TSV metal layer (such as voids, interface delamination, and cracks at connection points). And the 1dB compression point (P1dB) becomes smaller (i.e., the maximum power of linear operation decreases, and nonlinear effects become more pronounced); 2) Increased leakage current due to defects in the TSV insulation layer (poor coverage, contamination, and via wall defects, etc.); 3) S-parameter anomalies caused by defects in TSV substrate material, hole quality, and metallization quality.

b) Common failure modes in internal and external morphology evaluation include. 1) The structure and dimensions do not match the design; 2) TSV deformation and misalignment;

3) Cracks in the TSV three-dimensional structure; 4) Scratches or breaks in the metallization layer, residual metallization, or defects; 5) Metallization bulges and defects within TSVs with metal only on the sidewalls; 6) Filling metal voids within TSVs that are internally or partially filled with metal; 7) The insulation layer is discontinuous, delaminated, or porous; 8) Cracks, delamination, and voids at the interconnect interface; 9) Bond interface warping, gaps, metal overflow at the bond interface, etc.

c) Common failure modes in thermal stress characteristic evaluation include. cracking of silicon bulk or insulating layer caused by material thermal mismatch, interface delamination, and metal... Protrusions, etc.

d) Common failure modes in electrical stress characteristic evaluation include. uneven electric field distribution and excessive current density caused by structural defects in the TSV. The standard leads to dielectric breakdown and electromigration failure.

e) Common failure modes in mechanical property evaluation include. product fatigue caused by the TSV three-dimensional structure under cyclic stress (vibration). Labor cracks, interface delamination, interconnect failures, cracks in silicon or insulating layers, etc.

f) Common failure modes in interconnect characteristic evaluation include. 1) Wire bond strength test values that do not meet requirements due to surface impurities or defects can, in severe cases, lead to metallization layer defects. Bubbles and peeling appeared; 2) The chip shear strength test value does not meet the requirements due to residual surface impurities or defects.

g) Common failure modes in three-dimensional structural evaluation include. 1) The flexural strength test value does not meet the requirements due to unreasonable TSV layout design or defects in the three-dimensional structure of the TSV; 2) The interlayer bonding strength test value does not meet the requirements due to uneven wafer bonding surfaces, residual interface impurities, etc. 3) The metal composition of the bonding surface does not meet the design requirements.

6.1.1 DC Resistance

6.1.1.1 Evaluation of DC Resistance DC resistance can be used to evaluate the quality of TSV interconnects. Due to the excellent conductivity of metallic materials, the DC resistance of TSVs is very small. When defects exist in a TSV, its DC resistance will increase, and it may even cause an open circuit. The evaluation requirements for the DC resistance of a TSV three-dimensional structure are shown in Table 2.

6.1.1.2 Reporting Requirements The report should include at least the following.

a) Name and address of the manufacturing unit, product name, batch number, etc.;

b) Test environment. temperature, humidity, cleanliness, etc.;

c) Test equipment. model, name, and serial number;

d) Sample quantity and distribution;

e) Test methods, criteria, test procedures and results, and test duration;

f) DC resistance value;

g) Failure analysis report (if any).

6.1.2 Leakage Current

6.1.2.1 Leakage Current Evaluation Leakage current can be used to evaluate the insulation of the TSV sidewall dielectric layer. The main indicators of dielectric layer integrity are dielectric layer continuity, absence of pinholes, and... Uniform thickness. When pinholes appear in the dielectric layer, the leakage current of the TSV to the substrate may increase, or even cause a short circuit. Theoretically, the TSV and the substrate... The resistance between the substrates should be infinite, and the leakage current should be zero. However, when pinholes appear in the TSV dielectric layer, the resistance decreases, and the leakage current increases. The requirements for evaluating leakage current in three-dimensional structures are shown in Table 3.

6.1.2.2 Reporting Requirements The report should include at least the following.

a) Name and address of the manufacturing unit, product name, batch number, etc.;

b) Test environment. temperature, humidity, cleanliness, etc.;

c) Test equipment. model, name, and serial number;

d) Sample quantity and distribution;

e) Test methods, criteria, test procedures and results, and test duration;

f) IV test curve;

g) Failure analysis report (if any).

6.1.3 S-parameters

6.1.3.1 Evaluation of S-parameters S-parameters can be used to evaluate the quality of TSV radio frequency transmission. A network analyzer, combined with a probe station testing system, is used to perform three-dimensional TSV testing. S-parameter measurements of the structure show that a larger aspect ratio reduces the constraints on the layout design required for TSV impedance matching, and improves the bandwidth, insertion loss, and inversion resistance of the TSV. The better the characteristics such as radiation loss and isolation, the better. The evaluation requirements for the S-parameters of the TSV three-dimensional structure are shown in Table 4. Figure

6.1.4 Nonlinearity