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GB/T 47082-2026

Test method for stacking faults in polished monocrystalline silicon carbide wafers

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Table of Contents

Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part

1.Structure and Drafting Rules of Standardization Documents". Drafting. Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents. This document was prepared by the National Technical Committee on Standardization of Semiconductor Equipment and Materials (SAC/TC203) and the National Semiconductor Equipment and Materials Standards Committee. It was jointly proposed and is under the jurisdiction of the Materials Subcommittee of the Chemical Technology Committee (SAC/TC203/SC2). This document was drafted by: Shandong Tianyue Advanced Technology Co., Ltd., Guangdong Tianyu Semiconductor Co., Ltd., and Hebei Puxing Electronics. Technology Co., Ltd., Nanjing Baishi Electronic Technology Co., Ltd., Nanjing Shengxin Semiconductor Materials Co., Ltd., Anhui Changfei Advanced Semiconductor Joint-stock company, Xi'an Longwei Semiconductor Co., Ltd., Zhejiang Jingyue Semiconductor Co., Ltd., Beijing Tianke Heda Semiconductor Co., Ltd. The company, China Electronics Compound Semiconductor Co., Ltd., Ningxia Chuangsheng New Material Technology Co., Ltd., and Tyco Tianrun Semiconductor Technology (Beijing) Co., Ltd. The company is Xiamen Huaxin Wafer Semiconductor Co., Ltd. The main drafters of this document are. Zhang Hongyan, Chen Yanchang, Fu Jianxing, Yang Shixing, Song Sheng, Ding Xiongjie, Xue Hongwei, Hu Zhiwei, Han Xu, and Liu Hongchao. Ma Linbao, Ouyang Penggen, Gao Bing, She Zongjing, Pan Yaobo, Hu Huina, Liu Xiaoping, Chen Jisheng. Test method for stacking faults in silicon carbide single crystal polished wafers

1 Scope

GB/T 47082-2026 is the Chinese national standard covering stacking faults in a SiC wafer - the planar crystal defects that expand under forward current and progressively kill a power device, which makes them the defect the whole SiC industry is judged on. First edition, and

it belongs with the wafer geometry standards GB/T 43894.2-2026 and .3-2026 of the same period. It was issued on 28 January 2026 and has been in force since 1 August 2026, as a first edition. The document is under the responsibility of the Standardization Administration of China. This page is published from the official record of the 2026 edition; the clause text of a standard this recent is not yet in circulation, and the figures, limits and tables it contains are those of the document itself, delivered in full with the English translation.

2 Normative references

The contents of the following documents, through normative references within the text, constitute essential provisions of this document. Dated citations are not included. For references to documents, only the version corresponding to that date applies to this document; for undated references, the latest version (including all amendments) applies. This document.

GB/T 14264 Semiconductor Materials Terminology

GB/T 25915.1-2021 Cleanrooms and related controlled environments - Part

GB/T 30656 Polished silicon carbide single crystal wafers

GB/T 43612-2023 Defect Mapping of Silicon Carbide Crystal Materials

3 Terms and Definitions

The terms and definitions defined in GB/T 14264, GB/T 30656 and GB/T 43612-2023 apply to this document.

4.Principles Photoluminescence (PL) testing methods utilize excitation light sources with wavelengths smaller than the bandgap of SiC crystal materials (e.g.,...). The PL light signal obtained by irradiating a SiC single-crystal polished wafer with a wavelength of 313nm or 355nm is converted into an electrical signal by a photomultiplier tube, and then... The analog-to-digital converter processes the generated digital image and converts it into a grayscale image containing stacking fault features; or the PL light signal is processed through an image... Like a sensor converting a sensor image into a digital image, the digital image is processed to generate a grayscale image containing stacking fault features. Crystallographic data is then obtained through software analysis. The distribution and quantity of stacking faults were determined, and the samples were divided into grids according to usage requirements to calculate the area ratio of stacking faults.

5 Interference Factors

5.1 The stability of the light source power can affect the instrument's signal acquisition of stacking fault defects, which can easily lead to misjudgment during image analysis.

5.2 Strong vibration sources in the environment where the instrument is located can cause

instability in the optical path, affecting the accuracy of the test results.

5.3 Surface contamination of silicon carbide single crystal polished wafers can affect the results of stacking fault tests.

5.4 The settings of instrument software parameters, such as area threshold and sensitivity threshold, will affect the results of the number of stacking faults and the area ratio.

6 Test conditions

6.1 Test ambient temperature. 23°C±3°C.

6.2 Ambient relative humidity. 40%~70%.