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Semiconductor devices - Metallization stress void test

半导体器件 金属化空洞应力试验

(English Translation)

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Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents".

Drafting.

This document adopts IEC 62418:2010 "Testing for metallization voids in semiconductor devices".

This document adds two chapters. "Normative References" and "Terms and Definitions".

The following minimal editorial changes have been made to this document.

---Chapter 9 Formulas (2) to (4) have added explanations of the meanings of some letters and symbols.

Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents.

This document was proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

This document is under the jurisdiction of the National Semiconductor Device Standardization Technical Committee (SAC/TC78).

1 Scope

This document describes the testing methods and related criteria for void stress in aluminum (Al) or copper (Cu) metallization.

This document applies to reliability studies and qualification of semiconductor processes.

2 Normative references

This document has no normative references.

3 Terms and Definitions

This document does not contain any terms or definitions that need to be defined.

4 Test Equipment

The heating platform or chamber must be calibrated to ensure that the test structure of the wafer or package remains at the specified temperature for the specified time.

Within $\pm 5^{\circ}\text{C}$ deviation range. Specialized equipment is required for resistance measurement. For void detection, a stripping device to remove the scratch-resistant

protective layer and a scanning device are needed.

Scanning electron microscope (SEM).

5.1 Test Structure Graphics

All inspected metal layers use test structures, and several different types of structures can be used. This document specifies two test structures.

Note: For buried layer patterns in the test structure, if the metallization does not have a refractory shunt layer, reflection notches may appear at the steps, indicating relatively weak metallization.

The ability to withstand void stress.

5.2 Linear Graphics

Form a suitable test structure using parallel lines with the minimum linewidth allowed by the design. Unless otherwise specified, the minimum line length should be 500 μm , and the total length should be...

The length ranges from 1cm to 1000cm. Cavity stress is usually sensitive to the spacing between lines, so it is advisable to use a single, independent long line.

Note 1: Void stress is more likely to occur in narrow lines because the metal stress in narrow lines is usually higher than that in wide lines.

Note 2: The line length should be sufficient to form a hollow core.

5.3.1 Types of Graphics

Through-hole chain patterns can be used as test structures, or the Kelvin four-point measurement method can be used as a research technique.

5.3.2 AI process pattern

A through-hole chain consists of through-holes connected by lines of minimum linewidth, and the number of through-holes should preferably be between 1,000 and 100,000. Minimum linewidth should be used.