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Intelligent computing - Test methods for memristors - Part 2: Linearity

智能计算 忆阻器测试方法 第2部分：线性度

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Table of Contents

Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part

1.Structure and Drafting Rules of Standardization Documents". Drafting. This document is Part 2 of GB/T 46567 "Test Methods for Intelligent Computing Memristors". GB/T 46567 has published the following... part.

1.Basic Characteristics;

2.Linearity. Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents. This document was proposed by the National Intelligent Computing Standardization Working Group (SAC/SWG32). This document was prepared by the National Intelligent Computing Standardization Working Group (SAC/SWG32) and the National Semiconductor Device Standardization Technical Committee (SAC/ TC78) is under the same jurisdiction. This document was drafted by: Institute of Microelectronics, Chinese Academy of Sciences; Zhejiang Laboratory; Zhejiang University; and National University of Defense Technology of the Chinese People's Liberation Army. Hebei University, Northeast Normal University, Fudan University, the 13th Research Institute of China Electronics Technology Group Corporation, and Hangzhou Guolei Semiconductor Equipment Co., Ltd. Limited Liability Company, Shanghai Fudan Microelectronics Group Co., Ltd., China Academy of Information and Communications Technology, China Mobile (Hangzhou) Information Technology Co., Ltd., Inspur Electronic Information Industry Co., Ltd., China Telecom Cloud Technology Co., Ltd., China Mobile (Suzhou) Software Technology Co., Ltd., China Jiliang University, Shenzhen Luxi Technology Co., Ltd., Shenzhen Jiutian Ruixin Technology Co.,

Ltd., and Beijing Yunzhiyin Technology Co., Ltd. The main drafters of this document are. Wang Zhongxin, Xu Xiaoxin, Sun Wenxuan, Shi Tuo, Ma Xiaowen, Chen Peng, Wang Zhongqiang, Wang Ming, Yan Xiaobing, and Li Qingjiang. Zhong Xin, Liu Shanjia, Gu Hailin, Dong Hongliang, Huang Weijing, Zhang Jiuliu, Zhou Lan, Meng Guiyun, Zhang Lijing, Xu Haiyang, Li Ying, Liu Qi, Wang Yinan, Yang Biao Zhang Qian, Wang Binqiang, Zhang Mingming, Teng Yun, Yang Ming, Feng Jie, Liu Hailian, Zhou Peng, Liu Hongjie.

The resistance state of a memristor is determined by the external excitation history, possessing non-volatile memory functionality, making it ideal for achieving high-density, low-power, and fast data transfer. Memristors are ideal storage devices, providing a practical solution for developing high-efficiency in-memory computing systems. Simultaneously, memristors can simulate biological mutations. The synaptic behavior is applicable to the implementation of synaptic functions in deep neural networks (DNNs) and spiking neural networks (SNNs), providing a basis for neuromorphic computing. This laid the foundation for development. In cutting-edge applications such as neuromorphic computing, the performance of memristors directly impacts the overall system efficiency. Their key performance components... This includes fundamental characteristics (such as readout, electrical preprocessing, enhancement and suppression), linearity, impulse-dependent plasticity, and asymmetry. However, the current industry... The lack of unified testing method standards has led to a lack of comparability in performance evaluation results among different units, which has hindered the standardized development of the technology. To address this issue, it is urgent to establish scientific and systematic testing standards to ensure the objectivity and consistency of memristor performance evaluation. To respond to industry needs and promote technological standardization, GB/T 46567 "Test Methods for Intelligent Computing Memristors" is proposed to consist of four parts. constitute.

1.Fundamental Characteristics. This section describes the testing of fundamental characteristics of memristors, including read, electrical preprocessing, enhancement, and suppression. method.

2.Linearity. This section describes the testing methods for the linearity of memristors.

3.Pulse-dependent plasticity. The purpose is to describe the test method for the pulse-dependent plasticity of memristors.

4.Asymmetry. This section describes the test methods for memristor asymmetry. Intelligent computing memristor test method Part

2 Block diagram of memristor test device

5.1.2 Semiconductor Parameter Analyzer The semiconductor parameter analyzer should be able to provide synchronous measurement of current-voltage characteristics and capacitance-voltage characteristics through the source measurement unit and pulse

generation unit. The voltage characteristics and ultrafast pulse current-voltage characteristics should meet the requirements of Table 1.

5.1.3 Switch Matrix The switch matrix should have the ability to randomly combine input and output channels.

5.1.4 Probe Station The probe station should be able to make the probes contact the pins of the memristor under test, and the parameters should meet the requirements of Table 2.

3 Schematic diagram of memristor LTP test

6.1.2 Test Procedure During LTP operation, after each enhancement pulse is applied, a read voltage Vread is applied to read the memristor current. Vread should not cause... Unexpected resistance change in the memristor. The linearity test procedure for the memristor LTP operation is shown in Figure 4.

4 Device under Test

The memristor under test consists of an upper electrode, a resistive switching layer, and a lower electrode. Its structural schematic diagram and equivalent circuit diagram are shown in Figure 1a) and 1b, respectively. Figure 1b). During the read, preprocessing, enhancement, and suppression processes, different operating voltages Vpre will be applied to the upper and lower electrodes of the memristor. And Vpost.

5.1 Test Apparatus

5.1.1 Test Apparatus Block Diagram The block diagram of the memristor test device is shown in Figure

2.It mainly consists of a semiconductor parameter analyzer, a switch matrix, and a probe station. Figure

6.1 Linearity in the LTP process

6.1.1 Test Principle The principle of LTP testing is shown in Figure

3.During LTP operation, a repeated pulse with an amplitude of Vpo and a width of tpo needs to be applied to the upper electrode of the memristor. The lower electrode of the memristor is grounded. The current I is read by applying a read voltage Vread. After calculating the synaptic weight W of the memristor, the pulse is applied... Data processing yields the linearity of the LTP process of the device under test.

a) Schematic diagram of the memristor LTP test circuit

b) Timing diagram of LTP test voltage

Note. GND indicates grounding. Figure

6.2 Linearity in LTD Processes

6.2.1 Test Principle The LTD test principle is shown in Figure

5.During LTD operation, a repetitive pulse with amplitude Vde and width tde needs to be applied to the lower electrode of the memristor. A pulse is applied to ground the upper electrode of the memristor. The current I is read by applying a read voltage Vread, and the synaptic weight W of the memristor is calculated. Then, after... Data processing yields the linearity of the LTD process of the device under test.

6.2.2 Test Procedure During LTD operation, after each enhancement pulse is applied, a read voltage Vread is applied to read the memristor current. Vread should not cause... Unexpected resistance change in the memristor. The linearity test procedure for memristor LTD operation is shown in Figure 6.

6.2.3 Data Processing The ideal linear conductance during the LTD process is calculated using formula (5).

7 Test Report

The test report should include at least the following information.

a) Test personnel, test location, and test time;

b) Sample description, including memristor model/number, memristor structure (upper and lower electrodes and dielectric layer materials), sample dimensions (area,... thickness);

c) This document number;

d) Testing equipment, including equipment name, brand, and model;

e) A description of the test environment conditions, including at least ambient temperature, relative humidity, and atmospheric pressure;

f) LTP test results, including Vpo, tpo, Vread, WNmax_po, W0, Nmax_po, nset, kmax;

g) LTD test results, including Vde, tde, Vread, WNmax_de, W0, Nmax_de, nset, kmax;

h) Linearity test results, including Lpo and Lde;

i) Abnormal phenomena observed during the testing process. The test report template is in Appendix A.