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Specification for chiplet interconnection interface - Part 3: Data link layer technical requirements

芯粒互联接口规范 第3部分：数据链路层技术要求

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

This document is Part 3 of GB/T 46280 "Chiplet Interconnect Interface Specification". GB/T 46280 has been published in the following parts.

- Part 1: General provisions;

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- Part 2: Protocol layer technical requirements;

- Part 3: Data link layer technical requirements;

- Part 4: Physical layer technical requirements based on 2D packaging;

- Part 5: Physical layer technical requirements based on 2.5D packaging.

Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents.

This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

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Co., Ltd., China Science and Technology Integrated Circuit Co., Ltd., Shanghai Jiao Tong University, and Zhongyin Microelectronics (Nanjing) Co., Ltd.

The main drafters of this document are: Wu Huaqiang, Li Xiangyu, Zhang Yuqin, Cai Jing, Yang Lei, Cui Dong, Liu Haowen, Liu Zewei, Li Yang, Qi Xiao, Zhang Xu, Liu Qingsong, Li Nan, Wang Dapeng, Wang Wei, Ye Le, Jia Tianyu, Li Xinxi, Zhang Lai, Jin Peng, Wei Jinghe, Hua Songyi, He Guanghui, Jiang Jianfei, Yuan Chun, Zhu Hongwei, Xu Hongwen, and Gao Qiang.

Introduction

Chiplet technology is a technology that integrates multiple bare chips or integrated bare chips into one through high-bandwidth interconnect interfaces and advanced packaging.

Larger chips or systems have both high performance and low cost advantages. In the post-Moore era, chiplet technology is the key to supporting the development of the high-performance computing industry. One of the key technologies.

GB/T 46280 "Chip-to-Chip Interconnection Interface Specification" aims to unify the data transmission processing mechanism of point-to-point interconnection between chiplets, and is used for different Chips from the same supplier (design unit, manufacturing unit, packaging and testing unit), with different functions and different process nodes, can achieve efficient interconnection and interoperability.

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GB/T 46280 "Chip-Particle Interconnection Interface Specification" specifies the layered architecture of chip-particle interconnection, as well as the functional requirements of each layer and the interface between layers.

The requirements are to be composed of five parts.

- Part 1: General. The purpose is to define the terms and definitions, abbreviations of the chiplet interconnection interface, and to specify the classification of the chiplet interconnection interface.

The layer architecture and basic functions of each layer are defined, and the interconnection scenarios and encapsulation types are established.

- Part 2: Protocol layer technical requirements. The purpose is to specify the protocol layer technical requirements of the chiplet interconnect interface, general SoC bus protocol, high-bandwidth storage protocol, and custom protocol.

- Part 3: Data link layer technical requirements. The purpose is to specify the data link layer technical requirements of the chiplet interconnection interface.

- Part 4: Physical layer technical requirements based on 2D packaging. The purpose is to specify the physical layer technical requirements based on 2D packaging of chiplet interconnection interface.

Technical requirements for the management layer.

- Part 5: Physical layer technical requirements based on 2.5D packaging. The purpose is to specify the physical layer technical requirements based on 2.5D packaging of chiplet interconnection interfaces.

Physical layer technical requirements.

Chiplet Interconnect Interface Specification Part 3: Data link layer technical requirements

1 Scope

This document specifies the data link layer technical requirements for the chiplet interconnect interface, including. transmission message format, data error detection and correction mechanism control, as well as technical requirements related to link status and power consumption management.

This document applies to the design, manufacture and application of chiplet interconnect interfaces.

2 Normative references

GB/T 46280.1

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3 Terms and Definitions

The terms and definitions defined in GB/T 46280.1 apply to this document.

4 Abbreviations

The following abbreviations apply to this document.

Flit. data block (Flow control unit) IO. Input/Output port NRZ. Non-Return to Zero PHY. Physical layer RX. Receiver SoC. System on Chip TX. Transmitter

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