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Specification for chiplet interconnection interface - Part 1: General principles

芯粒互联接口规范 第1部分：总则

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

This document is Part 1 of GB/T 46280 "Chiplet Interconnect Interface Specification". GB/T 46280 has been published in the following parts.

- Part 1: General provisions;

- Part 2: Protocol layer technical requirements;

- Part 3: Data link layer technical requirements;

- Part 4: Physical layer technical requirements based on 2D packaging;

- Part 5: Physical layer technical requirements based on 2.5D packaging.

Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents.

This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

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This document was drafted by: Zhongguancun High-Performance Chip Interconnect Technology Alliance, China Electronics Technology Standardization Institute, Shenzhen HiSilicon Semiconductor Co., Ltd., Tsinghua University, Shenghejing Microsemiconductor (Jiangyin) Co., Ltd., Shenzhen ZTE Microelectronics Technology Co., Ltd., Peking University, China Mobile Communications Co., Ltd. Research Institute, Fujian Electronic Information (Group) Co., Ltd., Beijing Core Power Technology Innovation Center Co., Ltd.

Co., Ltd., China Science and Technology Integrated Circuit Co., Ltd., Shanghai Jiao Tong University, and Zhongyin Microelectronics (Nanjing) Co., Ltd.

The main drafters of this document are: Wu Huaqiang, Zhang Yuqin, Cai Jing, Cui Dong, Yang Lei, Li Xiangyu, Wu Bo, Wang Qian, Liu Zewei, Luo Duona, Wang Shiwei, Tang Liangxiao, Li Yang, Zhou Jun, Wang Haijian, Liu Haowen, Li Mingxuan, Qi Xiao, Huang Xinxing, Song Weixi, Xue Xingtao, Li Nan, Wang Dapeng, Wang Wei, Ye Le, Jia Tianyu, Li Xinxi, Zhang Lai, Jin Peng, Wei Jinghe, Hua Songyi, He Guanghui, Jiang Jianfei, Yuan Chun, Zhu Hongwei, Xu Hongwen, and Gao Qiang.

Introduction

Chiplet technology is a technology that integrates multiple bare chips or integrated bare chips into one through high-bandwidth interconnect interfaces and advanced packaging.

Larger chips or systems have both high performance and low cost advantages. In the post-Moore era, chiplet technology is the key to supporting the development of high-performance computing industry. One of the key technologies.

GB/T 46280 "Chip-Particle Interconnection Interface Specification" specifies the layered architecture of chip-particle interconnection, as well as the functional requirements of each layer and the interface between layers.

The requirements are aimed at unifying the data transmission processing mechanism of point-to-point interconnection between chips, which can be used by different suppliers (design units, manufacturing units, Packaging and testing units), chiplets with different functions and different process nodes achieve efficient interconnection and interoperability, and are planned to be composed of five parts.

- Part 1: General. The purpose is to define the terms and definitions, abbreviations of the chiplet interconnection interface, and to specify the classification of the chiplet interconnection interface.

The layer architecture and basic functions of each layer are defined, and the interconnection scenarios and encapsulation types are established.

- Part 2: Protocol layer technical requirements. The purpose is to specify the protocol layer technical requirements of the chiplet interconnect interface, general SoC bus protocol, high-bandwidth storage protocol, and custom protocol.

- Part 3: Data link layer technical requirements. The purpose is to specify the data link layer technical requirements of the chiplet interconnection interface.

- Part 4: Physical layer technical requirements based on 2D packaging. The purpose is to specify the physical layer technical requirements based on 2D packaging of chiplet interconnection interface.

Technical requirements for the management layer.

- Part 5: Physical layer technical requirements based on 2.5D packaging. The purpose is to specify the physical layer technical requirements based on 2.5D packaging of chiplet interconnection interfaces.

Physical layer technical requirements.

Chiplet Interconnect Interface Specification Part 1: General

1 Scope

This document defines the terms, definitions, and abbreviations of the chiplet interconnect interface, and specifies the layered architecture of the chiplet interconnect interface and the basic principles of each layer.

This function establishes interconnection scenarios and encapsulation types.

This document applies to the design, manufacture and application of chiplet interconnect interfaces.

2 Normative references

GB/T 9178

GB/T 14113

3 Terms and Definitions

The terms and definitions defined in GB/T 9178 and GB/T 14113 and the following apply to this document.

3.1 bare chip die

Unpackaged independent integrated circuit chips are obtained by dicing the wafer that has completed integrated circuit preparation.

3.2 chiplet

A bare chip or a Integrated bare chip.

Note. Usually has a certain degree of reusability, and multiple cores are integrated into an integrated circuit system through high-bandwidth interconnection.

3.3 2D package2D package

Traditional substrate-type flip chip (3.16) packaging format.

3.4 2.5D package2.5D package

A packaging form that can integrate multiple chips and components on the same substrate.

Note. Common packaging types include fan-out (3.17) organic interposer packaging, inorganic interposer (3.18) packaging, and embedded bridge packaging. form.

3.5 interconnect

The physical connection lines between core particles.