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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 45721.1-2025

**Semiconductor devices - Stress migration test - Part 1: Copper
stress migration test**

半导体器件 应力迁移试验 第1部分：铜应力迁移试验
(English Translation)

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

This document is part 1 of GB/T 45721 "Stress Migration Test for Semiconductor Devices". GB/T 45721 has been published as follows part.

--- Part 1: Copper stress migration test.

This document is equivalent to IEC 62880-1:2017 "Semiconductor device stress migration test standard Part 1: Copper stress migration test standard". The following minimal editorial changes were made to this document.

--- In order to coordinate with the existing standards, the name of the standard is changed to "Semiconductor Device Stress Migration Test Part 1: Copper Stress Migration Test test".

Introduction

Semiconductor devices are common basic products in the electronic industry chain and are the most basic units in electronic systems.

The "Stress Migration Test for Bulk Devices" series of standards are basic and universal standards for wafer-level testing of semiconductor devices.

The quality and reliability of core semiconductor devices at the wafer level play an important role. This series of standards is planned to consist of two parts.

--- Part 1: Copper stress migration test. The purpose is to evaluate the copper (Cu) metallization test structure on microelectronic wafers to stress induced Sensitivity to intravascular voiding (SIV).

--- Part 2: Aluminum stress migration test. The purpose is to evaluate the aluminum (Al) metallization test structure on the microelectronic wafer to stress induced The sensitivity of emptiness.

This series of standards is equivalent to the IEC 62880 series of standards, ensuring that the semiconductor device test methods are consistent with international standards and achieving semiconductor The device inspection method, reliability evaluation and quality level are in line with international standards. By formulating this series of standards, unified test methods and stresses are determined.

Evaluating the wafer-level reliability of semiconductor devices plays an important role in evaluating and assessing the quality and reliability of semiconductor devices, and also complements Improve the semiconductor device standard system and provide guidance for the development of the semiconductor device industry.

1 Scope

This document specifies a constant temperature aging method for testing the copper (Cu) metallization test structures on microelectronic wafers for stress The method will be mainly carried out during the wafer-level process development of the product, and the results will be used for lifetime prediction.

In some cases, this method can be applied to package level testing. Due to the long test time, this method is not suitable for product batch testing. One-time delivery inspection.

Dual Damascene copper metallization systems typically have a liner, such as tantalum (Ta) or nitride, at the bottom and sides of the trench etched into the dielectric layer.

Therefore, for a structure where a single through hole contacts a wide line below, the resistance drift caused by the void below the through hole reaches the failure criterion When the voltage reaches a certain percentage, it will instantly lead to open circuit failure.

2 Normative references

This document has no normative references.

3 Terms and definitions

The following terms and definitions apply to this document.

3.1

stress migration; SM An important failure phenomenon of semiconductor device interconnection.

Note: In semiconductor devices, factors such as mismatch of crystal structure or temperature change lead to uneven stress distribution in the crystal, thus causing stress in the crystal. Migration phenomenon.

3.2 Voids created in semiconductor device interconnects due to thermal stress

Note 1: In copper interconnects, voids can occur under or inside vias and cause increased resistance or open circuit failures.

Note 2: See Appendix A for the mechanism.

3.3 Wide pattern

Chain pattern, through-hole connection wide pattern.

Note: There are different combinations of connection methods. See Figure 1.

3.4 Nose pattern

A narrow, pattern connected to a via and connected to a wider, chain.

NOTE: The SIV risk of this through hole depends on the width of the board and the distance of the through hole from the board (see 4.1). See Figure 1. An example of the correlation between the nose shape and the geometric shape is shown in Appendix B.

3.5 Nose length

The length of the narrow part of the nose figure.

Note: See Figure 1.