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CCS L56

NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/T 44801-2024

Terminology of system in package (SiP)

系统级封装（SiP）术语

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part

1.Structure and drafting rules for standardization documents" Drafting. Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents. This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China. This document is under the jurisdiction of the National Technical Committee for Standardization of Integrated Circuits (SAC/TC599). This document was drafted by: China Electronics Technology Group Corporation No.

29 Research Institute, Chinese Academy of Sciences Institute of Microelectronics, Tsinghua University, Fudan University, Tianshui 749 Electronics Co., Ltd., and Chizhou Huayu Electronics Technology Co., Ltd. The main drafters of this document are. Ji Xingqiao, Yu Huihui, Jia Songliang, Wan Lixi, Lu Yinquan, Wu Yilong, Luo Jianqiang, Lu Qian, Peng Yong, Li Yanrui, Zeng Ce, Xu Rongqing, Xiang Weiwei, Dong Le, Lai Jinming, Li Xizhou, Qu Xinping, Pan Yuhua, Dai Xiaoli, Lü Yingfei, Li Yue, Li Meng, Lü Shuanjun, and Gao Feng. System-in-Package (SiP) Terminology

1 Scope

GB/T 44801-2024 defines the vocabulary of system in package. As transistor scaling has slowed, more of the progress in electronics has moved into packaging: putting several dies - logic, memory, radio, sensors - into one package and connecting them there, with stacked die, interposers, through-silicon vias, fan-out wafer level packaging and chiplets. The terminology grew with the techniques and grew inconsistently, and packaging is a field where the supply chain is long and the same physical structure is described differently by the foundry, the assembly house, the test house and the customer. This document defines the general and specific terms of system in package relating to materials, processes, assembly and packaging, across manufacturing, engineering application and product

testing. It applies to production, scientific research, teaching and trade in the system in package field. Under ICS 31.200 and CCS L56, it is written for semiconductor assembly and test providers, for the design houses specifying a package, and for the procurement and quality functions that have to read a datasheet from one company and a purchase specification from another and know they describe the same thing.

This document defines the system-level package (SiP) in terms of manufacturing, engineering application and product testing and other aspects related to materials, processes, assembly, packaging Related general and specific terms. This document is applicable to applications in production, scientific research, teaching, and trade related to system-level packaging.

2 Normative references

This document has no normative references.

3 General terms

3.1 System in package; SiP A system or subsystem that integrates multiple functional chips, packages, or a combination thereof into a single package, which may optionally contain passive components. components, micro-electromechanical systems (MEMS), optical components, and other packaging and devices.

Note. SiP generally integrates a system or subsystem into a single package.

3.2 System on package (SoP) Integrate components, packages, systems, or subsystems into a single package.

Note. SoP is a package that integrates multiple systems or subsystems in a single package. Its characteristic is that passive components are integrated in the substrate in the form of thin films.

3.3 System on chip systemonchip;SoC Integrate a complete system or subsystem on a single chip.

Note. Generally includes a microprocessor and its analog IP core or digital IP core or memory or off-chip storage control interface, etc.

3.4 Through micro-nano manufacturing technology, the integration of different materials, different processes, different structures and different functional units can be achieved.

3.5 An integrated circuit formed by combining any semiconductor integrated circuit and a film integrated circuit, or by combining any of these circuits with discrete components. [Source: GB/T 12842-1991, 2.1.11]

3.6 Multi-chip module multi-chipmodule; MCM Multi-chip modules A hybrid integrated circuit has two or more ultra-large-scale integrated circuit bare chips installed inside.

3.7 Multi-chip package multi-chippackage; MCP A package that contains multiple integrated circuits.