ICS 31.200
CCS L 55

NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/T 44791-2024

Integrated circuit 3D packaging-Requirement for bumping-wafer-thinning process and evaluation

集成电路三维封装 带凸点圆片减薄工艺过程和评价要求

Issued on: October 26, 2024 **Implemented on: May 1, 2025**

Issued by: State Administration for Market Regulation;
Standardization Administration of the PRC

Table of Contents

Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents.

This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

This document is under the jurisdiction of the National Technical Committee for Standardization of Integrated Circuits (SAC/TC599).

This document was drafted by the 58th Research Institute of China Electronics Technology Group Corporation and Shenzhou Loongson Intelligent Technology Co., Ltd.

The main drafters of this document are Yuan Shiwei, Wang Bo, Xiao Hanwu, Wang Yanting, Huang Hailin, Xiao Longteng, and Chen Mingmin.

Thinning process of wafer with bumps for integrated circuit 3D packaging Process and evaluation requirements

1 Scope

This document specifies the thinning process for 12-inch and below integrated circuit 3D packaging with bump wafers (hereinafter referred to as thinning process) Process and evaluation requirements.

This document is applicable to bumped wafers of 12 inches or less that need to be thinned. Note. 1 in = 2.54 cm.

2 Normative references

GB/T 25915.1-2021

3.1 Terms and Definitions

The following terms and definitions apply to this document.

3.1.1 Roughness

The micro-geometric characteristics of the thinned surface are composed of small spacing and peaks and valleys.

3.1.2 damaged layer

The outermost layer is a rough and broken surface structure, and the middle area is the

cracks caused by the outermost layer and its cracks.

The inner part is composed of extended microcracks, and the inner part is the elastic deformation area extending from the microcrack extension area.

Note. The schematic diagram of the damaged layer is shown in Figure 1.

Figure 1 Schematic diagram of the damaged layer