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NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/T 44777-2024

Guideline for intellectual property (IP) core protection

知识产权（IP）核保护指南

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part

1.Structure and drafting rules for standardization documents" Drafting. Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents. This document is

proposed by the Ministry of Industry and Information Technology of the People's Republic of China. This document is under the jurisdiction of the National Technical Committee for Standardization of Integrated Circuits (SAC/TC599). This document was drafted by: Harbin Institute of Technology, Hefei University of Technology, and China Electronics Standardization Institute. The main drafters of this document are. Xiao Liyi, Fu Fangfa, Wang Yongsheng, Wang Jinxiang, Lai Fengchang, Yin Yongsheng, Du Gaoming, Luo Xiaoyu, and Li Kun. Intellectual Property (IP) Core Protection Guide

1 Scope

GB/T 44777-2024 gives guidance on protecting semiconductor IP cores. An IP core is delivered as design data - RTL, a netlist or a hard macro - to a customer who must be able to build it into a chip while being prevented from reusing it in the next one, and the licensor cannot inspect what happens after delivery, so protection has to be built into the deliverable itself. The standard sets out the protection scheme in two halves. The legal half covers patents, copyright, trade secrets and the integrated circuit layout design right, with recommendations on which applies to what. The technical half covers encryption, protection by abstraction of the model, obfuscation, watermarking and fingerprinting for tracing a leak, hardware locking and activation, together with the management practices that support them. It took effect on 26 October 2024.

This document provides several intellectual property (IP) core protection plans and strategies, including legal protection means, technical protection means and detection Tracking methods. This document is intended for IP core providers and IP core users to refer to for selecting appropriate IP core protection and management solutions. Protection of electronic design automation (EDA) tools used in the IP core design process.

2 Normative references

This document has no normative references.

3 Terms and Definitions

The following terms and definitions apply to this document.

3.1 A predefined, verified, reusable component that can perform certain functions. IP core, solid IP core and hard IP core. [Source: GB/T 43452-2023, 3.1, with modifications]

3.2 Soft IP core Use hardware description languages such as Verilog or VHDL to write the functions required by the system into registers according to the established rules.

3.3 Firm IP core firmIPcore Components that have been optimized for performance and area in terms of structure and topology through place and route, or by leveraging a common process library.

Note. Usually includes synthesizable RTL files, reference technology libraries, detailed layout and complete or partial netlist. When it is a complete netlist, it is inserted The test logic is added and the test list is included in the design. The IP core does not include routing.

3.4 Hard IP core hard IP core Based on the solid IP core, power consumption, area and performance are optimized and mapped to a specific process.

Note. Generally expressed in GDSII format.

3.5 IP core provider IPcoreprovider The entity that creates and provides IP cores during the IP core transaction process.

Note. The IP core provider will provide relevant information and services of the IP core. [Source: GB/T 43452-2023, 3.2]