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Integrated circuit 3D packaging-Requirement for die stack process and evaluation

集成电路三维封装 芯片叠层工艺过程和评价要求

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Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

Please note that some of the contents of this document may involve patents. The issuing organization of this document does not assume the responsibility for identifying patents.

This document is proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

This document is under the jurisdiction of the National Technical Committee for Standardization of Integrated Circuits (SAC/TC599).

This document was drafted by the 58th Research Institute of China Electronics Technology Group Corporation and Shenzhou Loongson Intelligent Technology Co., Ltd.

The main drafters of this document are Yuan Shiwei, Gao Nayan, Xiao Hanwu, Shuai Zhe, Huang Hailin, Xiao Longteng, and He Huiying.

Integrated circuit 3D packaging Chip stacking process and evaluation requirements

1 Scope

This document specifies the chip stacking process and evaluation using wire bonding and flip chip technology in integrated circuit 3D packaging. Require.

This document applies to circuits stacked using wire bonding and flip-chip processes in integrated circuit three-dimensional packaging.

2 Normative references

GB/T 25915.1-2021

GB/T 35005-2018

3 Terms and Definitions

The following terms and definitions apply to this document.

3.1 Chip stacking diestack

Horizontal integration of chips containing two or more layers of active electronic devices into a single circuit.

4.1 Equipment, instruments and fixtures

The equipment and instruments required for the lamination process should be regularly identified and calibrated. The fixtures should be intact and clean, and the specifications and dimensions should be consistent with the process requirements.

In order to adapt to the requirements, the commonly used equipment, instruments and fixtures are shown in Table 1.

Table 1 Commonly used equipment, instruments and fixtures Serial No. Name Main Technical Requirements Application 1 Mounting machine chip accuracy. XY no more than 20μm, rotation less than or equal to 0.5° dispensing and mounting process 2 The temperature and pressure range of the hot press welder are adjustable for flip chip interconnection 3 The temperature error of the curing oven shall not exceed 10°C; the time error shall not exceed 5s within 30min.

4 Reflow oven temperature adjustable for solder paste welding and glue curing

5 No flux residue on the chip surface after cleaning by the cleaning machine. Cleaning the flip chip flux.

6 Low-power microscope meets the requirements for microscopic examination and appearance inspection after mounting