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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 43894.2-2026

**Practice for determining semiconductor wafer near-edge
geometry - Part 2: Roll-off amount (ROA)**

半导体晶片近边缘几何形态评价 第2部分：边缘卷曲法（ROA）

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Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part

1. Structure and Drafting Rules of Standardization Documents". Drafting. This document is Part 2 of GB/T 43894, "Evaluation of Near-Edge Geometry of Semiconductor Wafers". GB/T 43894 has been published. The following section.

1. The Method of Height Radial Second Derivative (ZDD);

2. Edge Curling (ROA) Method Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents. This document was prepared by the National Technical Committee on Standardization of Semiconductor Equipment and Materials (SAC/TC203) and the National Semiconductor Equipment and Materials Standards Committee. It was jointly proposed and is under the jurisdiction of the Materials Subcommittee of the Chemical Technology Committee (SAC/TC203/SC2). This document was drafted by: Shandong Advanced Semiconductor Materials Co., Ltd., Xi'an Yiswei Materials Technology Co., Ltd., and Tianjin Zhonghuan Ling. First Materials Technology Co., Ltd., Jinruihong Microelectronics (Quzhou) Co., Ltd., Zhejiang Lishui Zhongxin Wafer Semiconductor Technology Co., Ltd., Guangdong Tian Domain Semiconductor Co., Ltd., Shenzhen Zhongke Feice Technology Co., Ltd., and Yunnan Chihong International Germanium Co., Ltd. The main drafters of this document are: Ning Yongduo, Zhu Xiaotong, Yu Yadi, Wang Yue, Zhang Wanwan, Zhang Xuenü, Liu Yunxia, Xu Guoke, Lü Ying, and Xu Xinhua. Ding Xiongjie, Ma Yanzhong, and Lu Zhanqing.

As silicon wafer diameters increase and linewidths decrease, the requirements for silicon wafer geometry are also constantly increasing. The near-edge region of the silicon wafer... The region is a crucial factor influencing the geometric parameters of silicon wafers. Currently, controlling the thickness, flatness, and other morphological properties of the near-edge region of large-diameter silicon wafers is quite challenging. Therefore, effectively evaluating and controlling the near-edge geometry of large-diameter silicon wafers is crucial for improving the overall quality of silicon wafers and the yield of integrated circuit chips. Improving yield rates is of great significance for promoting technological upgrades. This series of standards is currently mainly used for silicon wafers and other semiconductor

material wafers. GB/T 43894, "Evaluation of Near-Edge Geometry of Semiconductor Wafers", is proposed to consist of four parts.

- 1.High Radial Second Derivative Method (ZDD). The aim is to evaluate the near-terminal properties of semiconductor wafers using the radial second derivative method. Edge geometry.
- 2.Edge Curl-up Method (ROA). The aim is to evaluate the near-edge geometry of semiconductor wafers using the edge curl-up method. form.
- 3.Sector Flatness Method (ESFQR, ESFQD, ESBIR). The purpose is to obtain the flatness of a sector area and then... Evaluate the geometry near the edge.
- 4.Local Smoothness Methods for Incomplete Regions (PSFQR, PSFQD, PSBIR). The purpose is to obtain the smoothness of incomplete regions. Local flatness is used to evaluate the near-edge geometry. This series of standards quantifies the geometric parameters of the near-edge region of the wafer using different calculation methods across different test areas. This document effectively evaluates and controls the near-edge geometry of the wafer. It incorporates years of testing and calibration experience. This is of great importance for developing large-diameter, high-quality semiconductor silicon wafers in my country and completely overcoming the backwardness in semiconductor materials and devices. The significance of. Evaluation of near-edge geometry of semiconductor wafers
Part

1 Scope

GB/T 43894.2-2026 is the Chinese national standard covering edge roll-off - the few nanometres by which a polished wafer droops away in its outermost millimetres, which decides how much of the wafer can be bonded, patterned or thinned without loss. Part 2 of the series, first edition of this part, with Part 3 on sector flatness. It was issued on 28 January 2026 and has been in force since 1 August 2026, as a first edition. The document is under the responsibility of the Standardization Administration of China. This page is published from the official record of the 2026 edition; the clause text of a standard this recent is not yet in circulation, and the figures, limits and tables it contains are those of the document itself, delivered in full with the English translation.

This document describes a method for evaluating the near-edge geometry of semiconductor wafers using the edge curling (ROA) method. This document applies to 300mm diameter polished silicon wafers, silicon epitaxial wafers, silicon-on-insulator (SOI) wafers, and other circular wafers with surface layers. This method is also applicable to the evaluation of the near-edge geometry of circular wafers made of other semiconductor materials.

Note. Refer to this document for.200mm diameter silicon wafers.

2 Normative references

The contents of the following documents, through normative references within the text, constitute essential provisions of this document. Dated citations are not included. For references to documents, only the version corresponding to that date applies to this document; for undated references, the latest version (including all amendments) applies. This document.

GB/T 14264-2024 Semiconductor Materials Terminology

GB/T 16596 Specification for Determining Wafer Coordinate Systems

GB/T 25915.1-2021 Cleanrooms and related controlled environments - Part

3 Terms and Definitions

The terms and definitions defined in GB/T 14264-2024, as well as the following terms and definitions, apply to this document.

3.1 center-referenced A coordinate system established with the center of the wafer as the origin, used for measurement and calculation.

3.2 edge-referenced A coordinate system established with a point on the periphery of the wafer as the origin, used for measurement and calculation. [Source: GB/T 14264-2024, 3.188]

3.3 Straight lines or three-dimensional curves are derived by fitting an ideal surface, excluding curling. [Source: GB/T 14264-2024, 3.189.9]

3.4 Reference segment The region used to fit the baseline.

4.Principles Height data arrays were acquired at different angles and in the radial direction. A baseline was fitted based on the edge curling data within the reference area, and the data were calculated one by one.