

ICS 31.200
CCS L 56



**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 43536.3-2026

**Three dimensional integrated circuits - Part 3: Model and
measurement methods of through-silicon via**

三维集成电路 第3部分：硅通孔模型及测试方法

(English Translation)

Issued on: July 30, 2026

Implemented on: February 1, 2027

Issued by: State Administration for Market Regulation

Table of Contents

Preface
Introduction
1 Scope
2 Normative References
3 Terms, Definitions, and Abbreviations
4 Test methods for characterizing TSV properties
Appendix A (Informative) Explanation

Foreword

Drafting.

This document is Part 3 of GB/T 43536 "Three-Dimensional Integrated Circuits". GB/T 43536 has already published the following parts.

---Part 1: Terms and Definitions;

---Part 2: Calibration Requirements for Micro-pitch Stacked Chips;

---Part 3: Through-Silicon Vias Model and Testing Methods.

This document is equivalent to IEC 63011-3:2018 "Integrated circuits - Three-dimensional integrated circuits - Part 3: Through silicon via modeling and testing".

Law".

The following minimal editorial changes have been made to this document.

---To align with existing standards, the standard name has been changed to "Three-dimensional integrated circuits, Part 3: Through-silicon via models and testing methods".

Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents.

This document was proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

This document is under the jurisdiction of the National Integrated Circuit Standardization Technical Committee (SAC/TC599).

Introduction

GB/T 43536 "Three-dimensional integrated circuits" is proposed to consist of three parts.

---Part 1: Terms and Definitions. The purpose is to standardize and guide the production, manufacturing, and application of multilayer chips using through-silicon via (TSV) technology.

---Part 2: Calibration Requirements for Micro-Pitch Stacked Chips. The purpose is to provide calibration requirements for stacked chips using through-silicon via (TSV) technology during manufacturing.

The vertical stacking calibration process provides an operable and verifiable procedure.

---Part 3: Through-Silicon Vias (TSV) Model and Testing Methods. The aim is to provide a reliable method for assessing the quality of chips using TSVs in multilayer packaging.

Standardization requirements.

3D Integrated Circuits Part 3: Through-Silicon Vias Model and Test methods

1 Scope

This document specifies an electrical characteristic reference model for through-silicon vias (TSVs) used for digital signal transmission and reception in 3D integrated circuits.

The paper describes the interface design of IC and the test methods for resistors and capacitors that characterize TSV properties in 3DIC.

The following three-dimensional integrated circuits are applicable to this document.

---Applications. Digital consumer and mobile devices;

---Operating voltage. 0.1V~5.0V;

---Operating frequency. less than 2.0GHz.

This document is not applicable to test equipment. Figure 1 is a typical example of a multi-chip interconnect system, used for the explanation of subsequent specifications.

Figure 1. Typical example of a multi-chip interconnect system

2 Normative references

The contents of the following documents, through normative references within the text, constitute essential provisions of this document. Dated citations are not included.

For references to documents, only the version corresponding to that date applies to this document; for undated references, the latest version (including all amendments) applies.

This document.

Note: GB/T 43536.1-2023 Three-dimensional integrated circuits - Part 1: Terms and definitions (IEC 63011-1:2018, IDT)

3.1 Terms and Definitions

The terms and definitions defined in IEC 63011-1 apply to this document.