

ICS 31.200
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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 43536.2-2023

**Three dimensional integrated circuits - Part 2: Alignment of
stacked dies having fine pitch interconnect**

三维集成电路 第2部分：微间距叠层芯片的校准要求

(English Translation)

Issued on: December 28, 2023

Implemented on: April 1, 2024

**Issued by: State Administration for Market Regulation, China National
Standardization Administration**

Table of Contents

Preface
Introduction
1 Scope
2 Normative references
3 Terms and Definitions
4 Calibration of chip bonding process
5 Calibration process
5.1 Bonding pre-calibration
5.2 Bonding calibration
5.3 Evaluation of calibration
Appendix A (Informative) Calibration Case
A:1 Calibration principle using capacitive coupling
A:2 Calibration principles using inductive coupling
A:3 Calibration measurement after stacking is completed
Reference

Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents" Drafting:

This document is Part 2 of GB/T 43536 "Three-dimensional Integrated Circuits": GB/T 43536 has released the following parts:

---Part 1: Terms and definitions;

---Part 2: Calibration requirements for fine-pitch stacked chips:

This document is equivalent to IEC 63011-2:2018 "Integrated circuits three-dimensional integrated circuits Part 2: Calibration of fine-pitch stacked chips Require":

This document has made the following minimal editorial changes:

---In order to coordinate with the existing standards, the name of the standard is changed to "Three-dimensional integrated circuits Part 2: Calibration requirements for fine-pitch stacked chips:" beg":

Please note that some content in this document may be subject to patents: The publisher of

this document assumes no responsibility for identifying patents:

Introduction

Through silicon via (TSV) technology is an innovative technology in three-dimensional integrated circuit applications: It can achieve high efficiency without reducing the feature size of the chip:

This enables the chip to achieve higher performance, better versatility and higher integration at the same time: GB/T 43536 "Three-dimensional integrated circuits" refers to it is a basic and universal standard that guides the three-dimensional stacked packaging process of integrated circuit chips in my country: It is planned to be developed by Composed of three parts:

---Part 1: Terms and definitions: The purpose is to define definitions related to multi-chip ICs:

---Part 2: Calibration requirements for fine-pitch stacked chips: The purpose is to manufacture stacked chips using through silicon via technology:

In-process vertical stack calibration gives an operational, verifiable procedure:

---Part 3: Through silicon via model and test method: The purpose is to provide reliable quality assurance for chip stack packaging using through silicon vias:

Standardized requirements:

3D Integrated Circuits Part 2:

Calibration requirements for fine pitch stacked chips

1 Scope

This document specifies the requirements for initial calibration and calibration maintenance between multiple stacked integrated circuits used during die bonding: Defined Calibration markings and procedures:

This document only applies to chip-to-chip calibration using electrical coupling methods:

2 Normative reference documents

The contents of the following documents constitute essential provisions of this document through normative references in the text: Among them, the dated quotations for undated referenced documents, only the version corresponding to that date applies to this document; for undated referenced documents, the latest version (including all amendments) applies to this document:

IEC 63011-1 Integrated circuits Three-dimensional integrated circuits Part 1: Terminology

(IntegratedCircuits-ThreeDimension-Note: GB/T 43536.1-2023 Three-dimensional integrated circuits Part 1: Terms and definitions (IEC 63011-1:2018, IDT)

3 Terms and definitions

The terms and definitions defined in IEC 63011-1 and the following apply to this document:

diebonding

Physical or chemical methods are used to achieve interconnection between chips:

bonderbonder

A device for bonding:

signalgeneratorsignalgenerator A device that generates electrical signals:

calibration mark alignmentkey Graphic for monitoring or adjusting multi-layer chip calibration:

Alignment tool aligner Device to perform calibration:

4 Calibration of chip bonding process

4.1

Calibration during stacking when the upper chip completely covers the lower chip, the calibration mark on the upper surface of the lower chip is invisible: Therefore, the lower chip can be first