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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 43536.1-2023

**Three dimensional integrated circuit - Part 1: Terminologies and
definitions**

三维集成电路 第1部分：术语和定义

(English Translation)

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Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents" Drafting:

This document is Part 1 of GB/T 43536 "Three-dimensional Integrated Circuits": GB/T 43536 has released the following parts:

---Part 1: Terms and definitions;

---Part 2: Calibration requirements for fine-pitch stacked chips:

This document is equivalent to IEC 63011-1:2018 "Integrated Circuits Three-dimensional Integrated Circuits Part 1: Terminology":

This document has made the following minimal editorial changes:

---In order to coordinate with existing standards, the name of the standard is changed to "Three-dimensional Integrated Circuits Part 1: Terms and Definitions":

Please note that some content in this document may be subject to patents: The publisher of this document assumes no responsibility for identifying patents:

Introduction

High-performance electronic systems require the exchange between big data processing integrated circuits (ICs) and storage ICs: Using vertical interconnect chips to stack multiple IC provides a higher data exchange rate between chips: In addition, traditional interconnects and TSVs such as bumps, metal pillars or metal pads can form integrated into three or more chips: There is a huge difference between a multi-IC integration environment and integration on a printed circuit board:

GB/T 43536 "Three-dimensional integrated circuits" is intended to consist of three parts:

---Part 1: Terms and definitions: The purpose is to define definitions related to multi-chip

ICs:

---Part 2: Calibration requirements for fine-pitch stacked chips: The purpose is to manufacture stacked chips using through silicon via technology:

In-process vertical stack calibration gives an operational, verifiable procedure:

---Part 3: Through silicon via model and test methods: The purpose is to provide reliable quality assurance for chip stack packaging using through silicon vias:

Standardized requirements:

Three-dimensional integrated circuits Part 1: Terms and definitions

1 Scope

This document defines the terms and definitions for multi-chip integrated circuits based on stacked chips implemented through silicon vias (TSVs) or bumps:

This document applies to the manufacturing and testing of multi-chip integrated circuits based on through-silicon vias (TSVs) or bumps to implement stacked chips:

2 Normative reference documents

This document has no normative references:

3 Terms and definitions

3.1

General terms

The following terms are related to the secondary integration method, which refers to the manufacturing method of vertically integrating integrated circuits on the horizontal surface of a semiconductor:

3.1.1

Adapter board interposer an interposer that connects one interface or interconnect layer to another:

Note: The purpose of the interposer board is to extend the interconnect layer to a wider pitch or to reroute to a different interconnect layer:

3.1.2

A technology that uses connection structures to stack basic electronic components between layers:

Note 1: "Basic electronic components" refers to transistors, diodes, resistors, capacitors, inductors,

etc:

Note 2: A special case of multi-chip interconnect technology is that the interposer board may contain only inner interconnect layers, although in many cases other electronic components (especially decoupling capacitors) can be embedded into the adapter board:

3.1.3

3-D bonding

The process of electrically or mechanically connecting two or more chip or wafer surfaces together:

Examples: chip-to-chip, chip-to-wafer, and wafer-to-wafer:

3.1.4

3D stacking 3-Dstacking A three-dimensional bonding operation that enables electrical interconnection between two or more devices:

3.1.5

3-D packaging

Multi-chip three-dimensional integration using wire bonding, stack-on-package or embedded in a printed circuit board:

3.1.6

Three-dimensional wafer-level packaging3-Dwafer-level-packaging;3-DWLP Wafer-level packaging technology used in three-dimensional integration:

Note: Including implementation after wafer manufacturing is completed, involving flip-chip redistribution, rewiring interconnection, fan-in packaging or fan-out reconfiguration wafer-level packaging: