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**NATIONAL STANDARD OF THE
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**Guideline for analog/mix-signal intellectual property(IP) core
document structure**

模拟/混合信号知识产权（IP）核文档结构指南

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Table of Contents

Preface	III
1 Scope	1
2 Normative references	1
3 Terms and Definitions	1
4 Description	2
5 Introduction to IP Core	2
5:1 Overview	2
5:2 Feature List	2
5:3 Functional block diagram	3
5:4 Port signal	3
5:5 Product information	3
5:6 Contact information	3
6 Functional Specifications	3
6:1 General	3
6:2 Introduction	3
6:3 Port description	4
6:4 Function description	5
6:5 Electrical Characteristics	5
7 Design Manual	5
7:1 General	5
7:2 Introduction	5
7:3 Architecture	6
7:4 Design methods and tool flow	8
7:5 Supplementary instructions	8
8 Functional and physical verification documentation	8
8:1 General	8
8:2 Introduction	8
8:3 Circuit level functional verification	9
8:4 Physical verification10	11
8:5 Post-simulation	11
8:6 Other instructions	12
9 Application Note	12

9:1 General	12
9:2 Introduction	12
9:3 Deliverable information ¹³	16
9:4 Functional and physical verification environment	16
9:5 Physical and process requirements	17
9:6 System integration	19
9:7 Design for testability	21
9:8 Other questions	22
Reference	23

Foreword

This document complies with the provisions of GB/T 1:1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents" Drafting:

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The main drafters of this document: Xiao Liyi, Fu Fangfa, Wang Yongsheng, Wang Jinxiang, Lai Fengchang, Yin Yongsheng, Du Gaoming, Luo Xiaoyu, and Li Kun: Analog/Mixed Signal Intellectual Property (IP) Core Document Structure Guide

1 Scope

This document provides the document structure related to the analog/mixed-signal intellectual property (IP) core, including IP core introduction, functional specifications, design manual, Functional and physical verification documentation and application manual:

This document is suitable for analog/mixed-signal IP core provider organizations to write analog/mixed-signal IP core-related documents, users and Quality control of third-party evaluation of analog/mixed-signal IP core documentation:

Note: The third party here refers to an independent institution that evaluates and provides services during the IP core transaction process:

2 Normative reference documents

This document has no normative references:

3 Terms and definitions

The following terms and definitions apply to this document: 3:1 Components that are defined in advance, verified, reusable, and capable of completing certain functions:

Core, solid core and hard core: [Source: GB/T 43452-2023,3:1] 3:2 IP core provider IP core provider The entity that creates and provides IP cores during the IP core transaction process:

Note: IP core providers will provide IP core related information and services: [Source: GB/T 43452-2023,3:2] 3:3 IP core user IP core user The entity that receives the IP core during the IP core transaction process:

Note: IP core users will complete the integration and reuse of IP cores, corresponding to IP core providers: [Source: GB/T 43452-2023,3:3] 3:4 important imperative IP core characteristics that need to be met:

Note: Failure to solve this problem when using IP cores for design will bring difficulties to the reuse of IP cores:

[Source: SJ/T 11479-2014,2:3, modified]