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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 43034.2-2024

**Integrated circuits - Measurement of impulse immunity - Part 2:
Synchronous transient injection method**

集成电路 脉冲抗扰度测量 第2部分: 同步瞬态注入法

(English Translation)

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Reference

Foreword

This document is in accordance with the provisions of GB/T 1.1-2020 "Guidelines for standardization work Part 1: Structure and drafting rules for standardization documents" Drafting.

This document is Part 2 of GB/T 43034 "Measurement of pulse immunity of integrated circuits". GB/T 43034 has been published as follows part.

--- Part 2: Synchronous transient injection method;

--- Part 3: Asynchronous transient injection method.

This document is equivalent to IEC TS62215-2:2007 "Integrated circuit pulse immunity measurement Part 2: Synchronous transient injection the document type was adjusted from IEC technical specifications to my country's national standards.

Introduction

To standardize the pulse immunity measurement of integrated circuits and provide pulse immunity measurement methods for integrated circuit manufacturers and testing institutions.

GB/T 43034 specifies the general conditions, definitions and test procedures for different injection measurement methods for integrated circuit pulse immunity measurements.

The test requirements are planned to consist of two parts.

--- Part 2: Synchronous transient injection method. The purpose is to specify the test procedures and test requirements of the synchronized transient injection method.

--- Part 3: Asynchronous transient injection method. The purpose is to specify the test procedures and test requirements for the asynchronous transient injection method.

Integrated circuit pulse immunity measurement Part 2: Synchronous transient injection method

1 Scope

This document gives general information and definitions for the test methods used to evaluate the immunity of integrated circuits (ICs) to fast conducted synchronous transient

disturbances.

This information includes test conditions, test equipment, test arrangement, test procedures and test report content requirements.

The purpose of this document is to describe the general conditions for obtaining quantitative measurements of IC immunity by establishing the same test environment.

Deviations from this document must be clearly noted in the test report.

The synchronous transient immunity test method given in this document is to use a fast rise time transient with different amplitude, duration and polarity.

The short pulse is coupled to the IC by conduction. In this method, the applied pulse needs to be synchronized with the functional operation of the IC to ensure controllable and reproducible conditions.

2 Normative references

This document has no normative references.

3 Terms and Definitions

The following terms and definitions apply to this document.

Auxiliary equipment auxiliary equipment; AE the non-permitted devices necessary to establish full functionality and determine correct performance (operation) of the device under test (DUT) when exposed to disturbances.

Test equipment.

coupling network A circuit with specified impedance and known transfer characteristics used to transfer energy from one circuit to another.

Device under test; DUT the device, equipment, or system being evaluated.

NOTE: In this document, DUT refers to the semiconductor device under test.

The equipment or system can work normally in its electromagnetic environment and does not cause any unacceptable electromagnetic disturbance to anything in the environment.

ability.

[Source. IEC 60050-161:1990, 161-01-07] 3.5 electrical noise Unwanted electrical signals that can produce harmful effects in the circuits of a control system.

[Source. IEEE std 100-1992-518-1982]