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NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

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Design requirements for radiation hardening of CMOS integrated circuits

CMOS集成电路抗辐射加固设计要求

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Table of Contents

Foreword

This document is in accordance with the provisions of GB/T 1:1-2020 "Guidelines for Standardization Work Part 1: Structure and Drafting Rules of Standardization Documents" drafted:

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This document is proposed and managed by the National Standardization Technical Committee of Aerospace Technology and Its Application (SAC/TC425):

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Radiation hardening design requirements for CMOS integrated circuits

1 Scope

This document specifies the process, design requirements, modeling and simulation, verification and design of CMOS integrated circuits for radiation resistance (total dose, single event) hardening design:

verification test requirements:

This document applies to digital integrated circuits, analog integrated circuits and digital-analog hybrid integrated circuits based on bulk silicon/SOICMOS process:

Radiation-resistant (total dose, single particle) rugged design:

2 Normative references

The contents of the following documents constitute essential provisions of this document through normative references in the text: Among them, dated citations

documents, only the version corresponding to that date applies to this document: For undated references, the latest edition (including all amendments) applies to this document:

GB/T 9178 Integrated Circuit Terminology

3 Terms, Definitions and Abbreviations

3:1 Terms and Definitions

The terms and definitions defined in GB/T 9178 and the following apply to this document:

totalionizingdoseeffects; TID

The total dose radiation effect refers to the phenomenon that the accumulation of ionizing radiation leads to the degradation of the parameters of the device:

single event effects; SEE

A single heavy ion or proton with a certain energy is injected into the integrated circuit, causing the integrated circuit to flip, lock, burn, etc:, resulting in the integrated circuit

A general term for the phenomenon of performance degradation or functional failure:

singleeventupseteffects; SEU

Effects of changes in the logic state of integrated circuits induced by single-event radiation:

singleeventtransienteffects;SET

The effect of an abnormal pulse signal at the output of an integrated circuit caused by single-event radiation:

Single event latch-up effects; SEL

The effect of integrated circuit latch-up caused by single event radiation:

Design reinforcement radiationhardeningbydesign; RHBD

The technology of improving the radiation resistance of semiconductor devices or integrated circuits by designing circuit topology and layout structure with radiation resistance: