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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 36614-2018

Integrated circuits -- Memory devices pin configuration

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- 3.1 Terms and definitions

Foreword

This standard was drafted in accordance with the rules given in GB/T 1.1-2009.

This standard uses the redrafting method to modify the use of IEC 61964..1999 "Integrated Circuit Memory Terminal Arrangement".

The technical differences between this standard and IEC 61964.1999 and their reasons are as follows.

---About the normative reference documents, this standard has made technical adjustments to adapt to China's technical conditions, adjustments

The situation is concentrated in Chapter 2, "Regulatory References", and the specific adjustments are as follows.

- * Replace IEC 60748 with GB/T 9178-1988;

- * Replace IEC 60748-1. 1984 with GB/T 16464-1996 equivalent to the international standard;

- * Added reference to GB/T 7092-1993.

---About terms, definitions and symbols, the specific adjustments are as follows.

- * References to the terms and definitions defined in the standard GB/T 9178-1988;

- * Added terms and definitions "or non-type flash memory (see 3.1.3.9)", "and non-type flash memory (see 3.1.3.10)",

"Dual in-line package (3.1.5.3)", "no lead-out chip package" (see 3.1.5.9), "thin double-sided flat no-lead end seal"

"" (see 3.1.5.7), "small outline package" (see 3.1.5.6), "small outline integrated circuit package" (see 3.1.5.4);

- * List the symbols individually to 3.2.

--- Removed 4.4, 4.5, 4.6 and 4.8 (see 4.4, 4.5, 4.6 and 4.8 of IEC 61964-1999);

--- Added Table 8 and Table 9.

This standard has made the following editorial changes.

--- The units of the device length and the lead end pitch in Tables 1 to 7 are modified into international units.

1 Scope

This standard specifies the arrangement of the terminals of the semiconductor integrated circuit memory.

This standard applies to nibble dynamic memory, word wide dynamic memory, byte wide dynamic memory, nibble synchronous dynamic memory, words

The arrangement of the strip width synchronous dynamic memory and the word width synchronous dynamic memory.

2 Normative references

The following documents are indispensable for the application of this document. For dated references, only dated versions apply to this article.

Pieces. For undated references, the latest edition (including all amendments) applies to this document.

GB/T 7092-1993 Dimensions of semiconductor integrated circuits

GB/T 9178-1988 Integrated circuit terminology

GB/T 16464-1996 Semiconductor device integrated circuits - Part 1. General (idt IEC 60748-1.1984)

3.1 Terms and definitions

The following terms and definitions as defined in GB/T 9178-1988 apply to this document.

3.1.1 Device Terminal

3.1.1.1

Address input address inputs; A(n)

Input Select one or a series of memory locations on the storage array to store data or send saved data to the device output.

The integer n is used to distinguish between different address inputs.

3.1.1.2

Address latch allows addresslatchenable; AL, AL\

Control the input signal of the terminal, the address input can be written to the register when it is true, and the input address state of the previous input is false.

Latch.

3.1.1.3

Storage block address bankaddress; BA

Control the terminal, use the storage block address in the read/write memory RAM with multiple memory block structures, and select it at any time.

One of the available storage blocks.

3.1.1.4

Column address columnaddress; CA

Controls the output, in a multiplexed dynamic memory DRAM, which is triggered by the column enable clock (CAS).

3.1.1.5

Column allows columnenable; CAS, CAS\

The enable signal excites column-related internal circuitry and data input/output circuitry in certain dynamic memory DRAMs. Device requirements

CAS\ will be valid when the RAS\ signal appears. In some new devices, RAS\signal and CAS\signal specific sequences are excited