



**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 35010.6-2018

**Semiconductor die products -- Part 6: Requirements for
concerning thermal simulation**

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Foreword

GB/T 35010 "Semiconductor Chip Products" is divided into the following sections.

- Part 1. Requirements for procurement and use;
- Part 2. Data exchange format;
- Part 3. Guide to handling, packaging and storage;
- Part 4. Chip user and supplier requirements;
- Part 5. Electrical simulation requirements;
- Part 6. Thermal simulation requirements;
- Part 7. XML format for data exchange;
- Part 8. EXPRESS format for data exchange.

This part is the sixth part of GB/T 35010.

This part is drafted in accordance with the rules given in GB/T 1.1-2009.

This section uses the translation method equivalent to IEC 62258-6:2006 "Semiconductor chip products Part 6. Thermal simulation information requirements."

The documents of our country that have a consistent correspondence with the international documents referenced in this part are as follows.

- GB/T 35010.1-2018 Semiconductor chip products - Part 1. Requirements for procurement and use (IEC 62258-1:2009,

IDT)

--- GB/T 35010.2-2018 Semiconductor chip products - Part 2. Data exchange format (IEC 62258-2..2009, IDT)

This section has made the following editorial changes.

--- Considering the adaptation to China's standard system, the name was changed to "Semiconductor chip products Part 6. Thermal simulation requirements."

1 Scope

This part of GB/T 35010 is used to guide the production, supply and use of semiconductor chip products. Semiconductor chip products include.

- * Wafer;
- * a single bare chip;
- * chips and wafers with interconnect structures;
- * Minimal or partially packaged chips and wafers.

This section specifies the required thermal simulation information to facilitate the use of electronic system thermal behavior and functional verification simulation models. electronic

The system includes a semiconductor bare chip with or without an interconnect structure, and/or a minimally packaged semiconductor chip. This part is to make the chip

All aspects of the supply chain meet the requirements of IEC 62258-1 and IEC 62258-2.

2 Normative references

The following documents are indispensable for the application of this document. For dated references, only dated versions apply to this article.

Pieces. For undated references, the latest edition (including all amendments) applies to this document.

IEC 62258-1 Semiconductor chip products - Part 1. Requirements for procurement and use (Semiconductor die products-Part 1.

Requirements for procurement and use)

IEC 62258-2 Semiconductor chip products - Part 2. Data exchange format (Semiconductor die products - Part 2.

Exchanged data formats)

3 Terms, definitions and abbreviations

Terms, definitions and abbreviations defined in IEC 62258-1 apply to this document.

4 General

According to IEC 62258-1, the chip product supplier shall provide a complete data package, which shall include the user in the design, procurement,

Necessary and sufficient information required for each stage of manufacturing and testing.

At the same time, most of the information provided should comply with relevant standards and be published in the public domain, and the information source can be in the manufacturer data form.

The form is traced back, but the manufacturer is not required to assume the obligation to disclose information. Any patent or business sensitive information that manufacturers can take

Protected by non-disclosure.

The requirements and recommendations provided in this section apply to the thermal simulation model. Model for analyzing thermal drift in chips for chip and system electrical

The impact of energy.

5.1.1 Overview

This clause includes requirements for bare chips with or without interconnect structures. The following information is to meet a specific thermal simulation model

Minimum requirements for information.

5.1.2 Working temperature conditions

The operating temperature range of the product should be provided.

5.1.3 chip maximum junction temperature

The maximum junction temperature allowed by the chip should be provided.

5.1.4 Extended junction temperature range

When the temperature exceeds the maximum junction temperature, the product life will be reduced compared to the operating temperature under 5.1.2, which should be applicable.

Description of the occasion.

5.1.5 Power dissipation

The maximum power dissipation value, minimum power dissipation value, and typical power dissipation value under specified conditions shall be provided.

5.1.6 Heat source distribution

When applied, the surface temperature field of the chip should be provided and the location and area of the heat source area should be indicated.

5.1.7 Heat source type and power

Each heat source type and power should be provided, including surface heat sources or body heat sources.

5.1.8 Thermal conductivity

The thermal conductivity of the various materials should be provided.

5.1.9 specific heat capacity

For transient simulations, the specific heat capacity of all materials should be provided.

5.2.1 Overview

This article, as provided in 5.1, shall provide the information defined in the following clauses.

The modeling method of the packaged product should be appropriate for that product type.

5.2.2 Package Thermal Resistance

The junction thermal resistance of the junction-environment or (and) junction-reference plane should be provided.

5.2.3 Thermal resistance measurement - test methods and conditions

Test methods and conditions for thermal resistance measurements (including ambient temperature and airflow, reference temperature and reference position) and measurement of thermal resistance should be provided

The power applied to the product.

5.2.4 Thermal properties of packaging materials

Thermal properties of all materials used to encapsulate the chip (eg, sealants, adhesives, insulating substrates, etc.) should be provided.