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NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/T 26067-2010

Standard test method for dimensions of notches on silicon wafers

硅片切口尺寸测试方法

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Foreword

The standard equipment by the National Standardization Technical Committee and the Technical Committee material of the semiconductor material (SAC/TC203/SC2) centralized. This standard was drafted. Grinm Semiconductor Materials Co., universal silicon peak Electronics Co., Ltd. The main drafters of this standard. Du, Sun Yan, Lu Liyan, Chunlan floor. Wafer size cut test methods

1 Scope

GB/T 26067-2010 is the Chinese national standard on standard test method for dimensions of notches on silicon wafers, in the field of electrical engineering. The /T suffix marks it as a recommended standard: it is not compulsory by itself, but it becomes binding as soon as a contract, a tender or a customer specification calls it up - which in practice is how most foreign buyers meet it. It was issued on 10 January 2011 by the General Administration of Quality Supervision, Inspection and Quarantine of the People's Republic of China; Standardization Administration of China, and has been in force since 1 October 2011. Classification: ICS 29.045, CCS H80. This page is published from the official record of the standard held by the Chinese standards administration: the identification, the dates, the classification and the issuing body are taken from there. The clause text, the tables and the numeric limits are in the document itself, which is delivered complete in English translation.

1.1 standard provides a qualitative determination of silicon reference notches meets the standard requirements of the limits of non-destructive testing methods. This method Test measurement principle equally applicable to other incision size.

1.2 standard size of 0.1mm when the object plane, passed 20 times magnification 2.0mm image will be formed on the projection screen pass Will produce 5.0mm over the projected 50-fold magnification. This method can be found in the smallest details of the size of the cut contour.

1.3 This standard does not provide a test cut to the top of the radius of curvature.

2 Normative references

The following documents for the application of this document is essential. For dated references, only the dated version suitable for use herein Member. For undated references, the latest edition (including any amendments) applies to this document.

GB/T 2828.1 Sampling procedures for inspection - Part 1. by acceptance quality limit (AQL) retrieval batch inspection sampling plan

GB/T 14264 semiconductor material terms

3 Terms and Definitions

Terms and definitions GB/T 14264 apply to this document defined.

4 Summary of Method

4.1 method is to use a series of contour cutout template on the screen and the projector projection on the stage of the wafer under test is compared, thus Get tested wafer notch meets the specified requirements.

4.2 silicon wafers cut edge of the wafer position locating projection and positioning pin projection tangent. At this time, the projection of the incision should be located in the bottom or lower A template to cut and depth has been set baseline projection and edge of the wafer at or above the contour plate in addition a baseline.

4.3 repositioning wafer with the wafer edge and contour templates "wafer peripheral line" coincidence, then cut the bottom of the projector should be in outline mode Board cut line between the deepest and most shallow incision line. A series of cuts and incisions on the projection angle of the angle cut edge contour of the template compared to 4.4, and wherein the selected template contour cut edges The best fit the corner angle as the angle of the cut.

4.5 can also use the instrument to cut the shape of the edge profile for accurate measurement, specific See Appendix A.

5 Disturbances

5.1 cut edges of any contamination or other rough material through the optical path of the projected image will produce distortion, resulting in an error is detected cut Port size.

5.2 cut position relative to the center of the wafer alignment is accurate cut parameters important part.

5.3 grinding tool wear and process variation could lead to the cut edge is not straight, so that the radius of the cut vertex is not unique. In this case, Next, with special attention to the

positioning cut the projected image in the correct position on the contour of the template.

5.4 in accordance with the specific crystal orientation tumbling edge of the wafer notch is formed on a silicon wafer method correctly positioned. Therefore, straight cut precision of critical dimension