ICS 29.045
CCS H80

NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

GB/T 16596-2019

Replacing GB/T 16596-1996

Specification for establishing a wafer coordinate system

确定晶片坐标系规范

Issued on: March 25, 2019 **Implemented on: February 1, 2020**

Issued by: State Administration for Market Regulation;
Standardization Administration of China

Table of Contents

Foreword

This Standard was drafted in accordance with the rules given in GB/T 1.1-2009. This Standard replaces GB/T 16596-1996 "Specification for establishing a wager coordinate system". Compared with GB/T 16596-1996, the main technical changes, except editorial changes, are as follows: -- In the "Normative references", delete GB/T 12964, SEMI M12 and SEMI M13, add GB/T 34479 and YS/T 986 (see Chapter 2, Chapter 2 of version 1996); -- Add "Establishing principle of a wafer coordinate system" (see Chapter 3); -- Add "Back wafer surface coordinate system" and "Three-dimensional coordinate system" (see 4.2, 4.3); -- Delete

4.1.2 of the "Application and related contents of the wafer coordinate system" (see 4.1.1,

4.1.2 of version 1996); -- Add contents such as "In SEMI M1, the edge reference coordinate system that is established with the edge contour template is used for edge reference, which is different from the wafer coordinate system. Edge contour template and edge contour parameters use different coordinate systems, as follows: ..." "In some cases, some wafer surfaces without patterns are difficult to be distinguished of front and back surfaces." "There is no special specification for the diameter of the wafer; however, for automatic equipment, only wafers of nominal diameter may be received" (see 5.3, 5.6, 5.9). This Standard is jointly proposed and managed by the National Semiconductor Equipment and Materials Standardization Technical Committee (SAC/TC 203) and the National Semiconductor Equipment and Materials Standardization Technical Committee Material Subcommittee (SAC/TC 203 / SC 2). The drafting organizations of this Standard: China Nonferrous Metals Techno- Economic Research Institute, GRINM Semiconductor Materials Co., Ltd., Zhejiang Haina Semiconductor Co., Ltd., Zhejiang Silicon Materials Quality Inspection Center, Wafer Works (Shanghai) Corp. The drafters of this Standard: Lu Liyan, Sun Yan, Pan Jinping, Yang Suxin, Lou Chunlan, Hu Jinzhi, Li Suqing. The previous versions of the standards which are replaced by this Standard are: -- GB/T 16596-1996. Specification for Establishing a Wafer Coordinate System

1 Scope

GB/T 16596-2019 is the Chinese national standard on specification for establishing a wafer coordinate system, in the field of electrical engineering. The /T suffix marks it as a recommended standard: it is not compulsory by itself, but it becomes binding as soon as a contract, a tender or a customer specification calls it up - which in practice is how most foreign buyers meet it. It was issued on 25 March 2019 by the State Administration for Market Regulation; Standardization Administration of China, and has been in force since 1 February 2020. Classification: ICS 29.045, CCS H80. This page is published from the official record of the standard held by the Chinese standards administration: the identification, the dates, the classification and the issuing body are taken from there. The clause text, the tables and the numeric limits are in the document itself, which is delivered complete in English translation.

This Standard specifies procedures for using rectangular coordinates and polar coordinates to establish the front, back, and three-dimensional wafer coordinate systems. This Standard applies to the establishment of wafer coordinate systems with and without pattern. The coordinate system is used to determine and record the exact locations of test results such as defects and particles on the wafer.

2 Normative references

The following documents are indispensable for the application of this document. For dated references, only the dated version applies to this document. For undated references, the latest edition (including all amendments) applies to this document.

GB/T 16595, Specification for a universal wafer grid

GB/T 34479, Specification for alphanumeric marking of silicon wafers YS/T 986, Specification for serial alphanumeric marking of the front surface of wafers SEMI E5, Specification for SEMI equipment communications standard 2 message content (SECS-II) SEMI M1, Specification for polished single crystal silicon wafers

3 Establishing principle of a wafer coordinate system

3.1 General The wafer coordinate system in this Standard uses the center point of the wafer as the origin of the rectangular coordinates (X-Y) or the polar coordinates (r-theta) to determine the coordinate of any point on the wafer. For a wafer without pattern, the wafer coordinate system can be used directly; it can also be used together with a rectangular array or a polar coordinate overlay array. The wafer coordinate system can also be used to determine the positions of the origin or other reference points of the other coordinate system, which often represents the wafer coordinate system. Edge contour template and edge contour parameters use different coordinate systems, as follows:

a) For the edge contour template, use the radial direction of the X-axis (inward from the wafer edge) and the vertical direction of the Y-axis (from the wafer surface to the wafer median plane) to define the template;

b) For the edge contour parameters, use the radial direction of the q-axis (inward from the wafer edge) and the vertical direction of the Z-axis (from the wafer median plane to the wafer surface) to define the cross section of the edge contour.

5.5 In SEMI E5, the standard position of the wafer is similar to its position in the wafer coordinate system, that is, the main positioning reference is downward, and its bisector is in the negative direction of the Y-axis; the rotational position of the wafer is defined by the clockwise rotation from the standard position, which is contrary to the polar coordinate rules of the wafer coordinate system. In SEMI E5, do not rotate the axis of the coordinate system; the wafer rotates relative to the axis. In the wafer coordinate system, the coordinate axes are positioned by the wafer itself, which is not limited by the actual spatial position of the wafer.

5.6 In GB/T 34479 and YS/T 986, for wafers with reference planes of diameters of 100 mm, 125 mm and 150 mm, the position of its character field is specified with reference to the reference plane, instead of the reference wafer center point; the position of the character field is varied with respect to the center point of the wafer; the coordinates of the position at the top corner of the character field (in the wafer coordinate system) may vary from wafer to wafer; the position of the character field of wafers with slits of diameters of 150 mm, 200 mm and 300 mm are positioned with reference to the wafer center point.

5.7 In some cases, some wafer surfaces without patterns are difficult to be distinguished of front and back surfaces.

5.8 SEMI E5 describes how a coordinate system reports position data that is to be transmitted in "Stream 12 - chip image". In addition, the origin of the coordinate system may be specified by the device when the wafer image is generated; it may also be one of five positions in the array (namely, upper left corner, lower left corner, upper right corner, lower right corner, or center). The "stream" ensures the transfer of any data of the wafer image coordinate system and the reference point corresponding to the actual wafer; and the wafer coordinate system can be used to determine the position of the reference point and the origin of the wafer image coordinate system.