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NATIONAL STANDARD OF THE PEOPLE'S REPUBLIC OF CHINA

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GB/T 16595-2019

Replacing GB/T 16595-1996

Specification for a universal wafer grid

晶片通用网格规范

Issued on: March 25, 2019 **Implemented on: February 1, 2020**

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Foreword

This Standard was drafted in accordance with the rules given in GB/T 1.1-2009. This Standard replaces GB/T 16595-1996, "Specification for a universal wafer grid". Compared with GB/T 16596-1996, the main technical changes, except editorial changes, are as follows: -- Add the scope of application "This Standard applies to silicon wafers of which the nominal diameter is 100 mm ~ 200 mm; it also applies to other semiconductor material wafers" (see Chapter 1); -- Include part of the contents of "Chapter 1, Scope", in "

5 Application of grids" (see Chapter 5, Chapter 1 of version 1996); -- Delete GB/T 1554, YS/T 209, SEMI M1, SEMI M2 and SEMI M11 in "Normative references"; add GB/T 30453 (see Chapter 2, Chapter 2 of version 1996); -- Modify the contents of

4.1.2 of "4.1, Grid cell plan", into "the selection of the grid outer diameter shall take into account the edge removal, diameter allowable deviation and chamfer of the wafer. Generally, the grid outer diameter is selected as the diameter of the qualified mass zone, wherein the radius of the qualified mass zone is 3 mm or 4 mm smaller than the nominal radius of the wafer; the corresponding grid circle diameter is shown in Table 2" (see 4.1.2,

4.1.2 of version 1996); -- Add grid circle diameters for wafers whose diameters are 150 mm and 200 mm, of which the qualified mass radius is 4 mm smaller than the nominal radius of the wafer (see Table 2); -- Modify the contents of the "4.4, Wafer with sub-reference plane" into "when a qualified mass area whose radius is 3 mm smaller than the wafer nominal radius is used, the grids will not exceed the edge of the wafer sub-reference plane area; therefore, the grid ignores the sub-reference plane" (see 4.4,

4.4 of version 1996); -- Add "

5 Application of grids" (see Chapter 5). This Standard is jointly proposed and managed by

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the National Semiconductor Equipment and Materials Standardization Technical Committee (SAC/TC 203) and the National Semiconductor Equipment and Materials Standardization Technical Committee Material Subcommittee (SAC/TC 203 / SC 2). The drafting organizations of this Standard: Zhejiang Haina Semiconductor Co., Ltd., China Nonferrous Metals Techno-Economic Research Institute, GRINM Specification for a Universal Wafer Grid

1 Scope

GB/T 16595-2019 is the Chinese national standard on specification for a universal wafer grid, in the field of electrical engineering. The /T suffix marks it as a recommended standard: it is not compulsory by itself, but it becomes binding as soon as a contract, a tender or a customer specification calls it up - which in practice is how most foreign buyers meet it. It was issued on 25 March 2019 by the State Administration for Market Regulation; Standardization Administration of China, and has been in force since 1 February 2020. Classification: ICS 29.045, CCS H80. This page is published from the official record of the standard held by the Chinese standards administration: the identification, the dates, the classification and the issuing body are taken from there. The clause text, the tables and the numeric limits are in the document itself, which is delivered complete in English translation.

This Standard specifies grid patterns that can be used to quantitatively describe surface defects on a circular semiconductor wafer. This Standard applies to silicon wafers of which the nominal diameter is 100 mm ~ 200 mm; it also applies to other semiconductor material wafers

2 Normative references

The following documents are indispensable for the application of this document. For dated references, only the dated version applies to this document. For undated references, the latest edition (including all amendments) applies to this document.

GB/T 6624, Standard method for measuring the surface quality of polished silicon slices by visual inspection

GB/T 12964, Monocrystalline silicon polished wafers

GB/T 14139, Silicon epitaxial wafers

GB/T 14142, Test method for crystallographic perfection of epitaxial layers in silicon. Etching technique

GB/T 14264, Semiconductor materials. Terms and definitions

GB/T 30453, Metallographs collection for original defects of crystalline silicon

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3 Terms and definitions

Terms and definitions determined by GB/T 14264 are applicable to this document.

4.1 Grid cell plan

4.1.1 The grid, which is positioned by the wafer center, defines two grids: one for the wafer without main reference plane (that is, the main positioning Figure 1 -- Grid diagram without main reference plane wafer

4.2 Wafer without main reference plane

4.2.1 The grid pattern without main reference plane wafer is shown in Figure 1. The grid pattern is drawn by concentric circles and radial division cells from the relative diameters that are specified in Table 1.

4.2.2 In Table 1, column 1 shows the circle numbers, 01~18; column 2 shows the division cell numbers on the outermost ring of the numbered circle; column 3 shows the division line angle; column 4 shows the total division cell number of the corresponding numbered circle; column 5 shows the area ratio that is included in the circle of corresponding serial number, the value of which is the total number of division cells that are contained in the circle divided by the total number of division cells of the grid 1 000; column 6 shows the relative diameter, the value of which is the square root of the included area ratio.

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