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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 15879.612-2025

**Mechanical standardization of semiconductor devices - Part 6-12: General rules
for the preparation of outline drawings of surface mounted semiconductor
device packages - Design guidelines for fine-pitch land grid array (FLGA)**

半导体器件的机械标准化 第6-12部分：表面安装半导体器件封装外形图绘制的一般规则 密节距焊盘阵列封装（FLGA）的设计指南

(English Translation)

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Foreword

This document complies with the provisions of GB/T 1.1-2020 "Standardization Work Guidelines Part 1: Structure and Drafting Rules of Standardization Documents".

Drafting.

This document is Part 6-12 of GB/T 15879 "Mechanical Standardization of Semiconductor Devices". GB/T 15879 has published the following...

part.

---Part 4: Classification and Coding System of Semiconductor Device Package Shapes;

---Part 5: Recommended values for tape-based automated bonding (TAB) of integrated circuits;

---Part 6-4.General Rules for Drawing Outline Diagrams of Surface Mount Semiconductor Device Packages Ball Array (BGA) Package Dimensions Measurement methods;

---Part 6-12.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages Close-Pitch Pad Array Packages (FLGA) design guidelines.

This document is equivalent to IEC 60191-6-12:2011 "Semiconductor devices - Mechanical standardization - Part 6-12.Surface mount semiconductors".

General rules for drawing device package outlines. Design guidelines for close pitch pad

array packages (FLGA).

Please note that some content in this document may involve patents. The issuing organization of this document assumes no responsibility for identifying patents.

The following minimal editorial changes have been made to this document.

---Added supplementary explanatory notes (see notes in Chapter 6, Figure 3, Figure 4, and Table 1);

---Added Appendix A (Informative). Outline diagram of FLGA plastic package with pads located inside the solder mask layer.

This document was proposed by the Ministry of Industry and Information Technology of the People's Republic of China.

This document is under the jurisdiction of the National Integrated Circuit Standardization Technical Committee (SAC/TC599).

Introduction

GB/T 15879 "Mechanical Standardization of Semiconductor Devices" is proposed to consist of 28 parts, corresponding to IEC 60191, mainly including...

Dimension symbols and definitions for semiconductor device outline drawings, drawing rules, package outline classification and coding system, and various types of semiconductor devices.

Outline drawing and recommended size range of the component package.

---Part 1: General Rules for Drawing Discrete Device Outlines. The purpose is to define the dimensional symbols used for drawing outlines of semiconductor discrete devices.

And definitions, drawing rules, and instances, etc.

---Part 2: Dimensions. This section specifies the dimensional requirements for various semiconductor device packages.

---Part 3: General Rules for Drawing Integrated Circuit Outlines. The purpose is to define the dimension symbol codes and...

Definitions, drawing rules, and instances, etc.

---Part 4: Classification and Coding System for Semiconductor Device Package Shapes. The purpose is to define the classification of semiconductor device package shapes.

Class, model naming and coding system.

---Part 5: Recommended values for automated tape-on-board (TAB) bonding of integrated circuits. The purpose is to specify the recommended values for automated tape-on-board

(TAB) bonding of integrated circuits.

Recommended package dimensions for the product.

---Part 6: General Rules for Drawing Outlines of Surface Mount Semiconductor Devices.
The purpose is to specify the outlines for surface mount semiconductor devices.

General requirements and rules for drawing package outline diagrams.

---Part 6-1.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages - Airfoil Lead Design Guidelines. The purpose is to...

The standard outline, dimensions, and recommended range values for the specified airfoil lead wires are provided.

---Part 6-2.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages 1.50mm, 1.27mm, 1.00mm Design guidelines for solder ball and post array packages with specific pitches. The aim is to specify solder ball and post array package design guidelines for 1.50mm, 1.27mm, and 1.00mm pitches.

Standard outlines, dimensions, and recommended range values for ball and pillar array packages.

---Part 6-3.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages Dimensions of Quad Flat Packages (QFP) Measurement methods. The purpose is to define the measurement methods for the dimensions of Quad Flat Packages (QFP).

---Part 6-4.General Rules for Drawing Outline Diagrams of Surface Mount Semiconductor Device Packages Ball Array (BGA) Package Dimensions Measurement methods. The purpose is to specify the measurement methods for the external dimensions of ball array packages (BGA).

---Part 6-5.General Rules for Drawing Outlines of Surface Mount Semiconductor Devices Close Pitch Ball Array (FBGA) Design Guidelines South. The purpose is to specify the standard outline, dimensions, and recommended range values for close-pitch ball arrays (FBGA).

---Part 6-6.General Rules for Drawing Outlines of Surface Mount Semiconductor Devices - Design Guidelines for Close Pitch Array of Pads (FLGA) South. The purpose is to specify the standard outline, dimensions, and recommended range values for closely spaced grid pad arrays (FLGA).

---Parts 6-8.General Rules for Drawing Outline Diagrams of Surface Mount Semiconductor Device Packages Glass-Sealed Ceramic Quad Flat Packages (G-QFP) Design Guidelines. The purpose is to specify the standard outline and dimensions of the glass-sealed ceramic quad flat package (G-QFP).

Inches and recommended range values.

---Parts 6-10.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages Thin Plastic, Small Outline, Leadless Packages the dimensions of (P-VSON) are specified. The purpose is to define the standard outline and dimensions of the very thin, small-form-factor, leadless plastic package (P-VSON).

Inches and recommended range values.

---Part 6-12.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages Close-Pitch Pad Array Packages the design guidelines for Fine Pitch Array (FLGA) packages aim to specify the standard outline, dimensions, and push-out parameters for Fine Pitch Array (FLGA) packages.

Recommended range values.

---Parts 6-13.Top Open Sockets for Close Pitch Ball Array Packages (FBGA) and Close Pitch Pad Array Packages (FLGA) the design guidelines aim to specify the top-end specifications for close-pitch ball array packages (FBGA) and close-pitch pad array packages (FLGA).

Standard outline drawing, dimensions, and recommended range values for open fixtures.

---Parts 6-16.Ball Array Package (BGA), Pad Array Package (LGA), Close Pitch Ball Array Package (FBGA), and Close Pitch Ball Array Package (FBGA) Glossary of semiconductor testing and aging sockets for pitch pad array packages (FLGA). The purpose is to define the terminology for ball array packages.

(BGA), LGA, FBGA, and FLGA.

Semiconductor testing and aging fixture terminology definitions.

---Part 6-17.General Rules for Drawing Surface Mount Semiconductor Device Package Outlines - Stack-up Package Design Guidelines - Close Pitch Ball Array Package (FBGA) and Close Pitch Pad Array Package (FLGA). The purpose is to define the Close Pitch Ball Array Package.

Standard outlines, dimensions, and recommended range values for (FBGA) and close pitch pad array (FLGA) packages.

---Part 6-18.General Rules for Drawing Outline Drawings of Surface Mount Semiconductor Device Packages Ball Array Package (BGA) Design Guidelines. The purpose is to specify the standard outline, dimensions, and recommended range values for ball array packages (BGA).

---Part 6-19.Measurement methods and maximum permissible warpage for packaged surfaces at high temperatures. The purpose is to specify the warpage of packages at high temperatures.