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**NATIONAL STANDARD OF THE
PEOPLE'S REPUBLIC OF CHINA**

GB/T 15879.604-2023

**Mechanical standardization of semiconductor devices - Part 6-4: General rules for the
preparation of outline drawings of surface mounted semiconductor device packages -
Measuring methods for package dimensions of ball grid array (BGA)**

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Standardization Administration**

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foreword

This document is in accordance with the provisions of GB/T 1:1-2020 "Guidelines for Standardization Work Part 1: Structure and Drafting Rules for Standardization Documents"

drafting:

This document is Part 6-4 of GB/T 15879 "Mechanical Standardization of Semiconductor Devices": GB/T 15879 has been issued with

Lower part:

--- Part 4: Classification and coding system of semiconductor device package appearance;

--- Part 5: Recommended values for integrated circuit tape automatic bonding (TAB);

--- Part 6-4: Dimensions of general rules for drawing surface-mounted semiconductor device package outline drawings for ball array (BGA) packages

Measurement methods:

This document is equivalent to IEC 60191-6-4:2003 "Mechanical Standardization of Semiconductor Devices - Part 6-4: Surface Mount Semiconductor Devices

General Rules for Drawing Component Package Outline Drawings Dimensional Measurement Methods for Ball Array (BGA) Packages:

Please note that some contents of this document may refer to patents: The issuing agency of this document assumes no responsibility for identifying patents:

Introduction

GB/T 15879 "Mechanical Standardization of Semiconductor Devices" is proposed to be composed of 28 parts, corresponding to the conversion of IEC 60191 series standards

Standards, mainly including dimension symbols and definitions for semiconductor device outline drawing, drawing drawing rules, package outline classification and coding system, and

Standard outline drawings and recommended size ranges of standard packages for various semiconductor devices:

--- Part 1: Semiconductor outline drawing: The purpose is to specify the dimension symbols and definitions for drawing the outline drawing of semiconductor devices, drawing

rules and examples etc:

--- Part 2: Dimensions: The purpose is to specify the external dimension requirements of various semiconductor device packaging products:

--- Part 3: General principles for drawing outline drawings of integrated circuits: The purpose is to specify the dimension symbol code and

Definition, drawing rules and examples, etc:

--- Part 4: Classification and coding system of semiconductor device package appearance: The purpose is to specify the classification of semiconductor device package outline

Class and model nomenclature and coding system:

--- Part 5: Recommended values for integrated circuit tape automatic bonding (TAB): The purpose is to specify the automatic soldering of integrated circuit tape

recommended package size for the product:

--- Part 6: General rules for drawing surface mount semiconductor device package outline drawings: The purpose is to specify the surface mount semiconductor

General requirements and rules for drawing device package outline drawings:

--- Part 6-1: General rules for drawing surface mount semiconductor device package outline drawing Wing lead design guidelines: The purpose is

Standard outline drawings, dimensions and recommended range values for specified wing leads:

--- Part 6-2: General rules for drawing surface mount semiconductor device package outline drawings 1:50mm, 1:27mm, 1:00mm sections

Ball and Pillar Array Package Design Guidelines for pitch: The purpose is to specify 1:50mm, 1:27mm, 1:00mm pitch solder balls

Standard outline drawings, dimensions and recommended range values for and post array packages:

--- Part 6-3: General rules for drawing surface mount semiconductor device package outline

drawings Dimensions of quad flat package (QFP)

Measurement methods: The purpose is to specify the measurement method of the quad flat package (QFP) external dimensions:

--- Part 6-4: Dimensions of general rules for drawing surface-mounted semiconductor device package outline drawings for ball array (BGA) packages

Measurement methods: The purpose is to specify the measurement method for the outline dimensions of ball array (BGA) packages:

--- Part 6-5: General rules for drawing surface mount semiconductor device package outline drawings Fine-pitch ball array package

(FBGA) size measurement method: The purpose is to specify the measurement method for the outline dimensions of fine-pitch ball array package (FBGA):

--- Part 6-6: General rules for drawing surface mount semiconductor device package outline drawings Fine-pitch land array package

(FLGA) size measurement method: The purpose is to specify the measurement of the outer dimensions of the fine-pitch land array package (FLGA)

method:

--- Part 6-7: General rules for dimensions of plastic very thin outline quad flat package (P-VQFN): The purpose is to stipulate the plastic

Standard dimensions and recommended range values for very thin outline quad flat package (P-VQFN):

--- Part 6-8: General rules for drawing surface mount semiconductor device package outline drawings Glass-sealed ceramic quad flat package

(G-QFP) Design Guidelines: The purpose is to specify the standard outline drawing and dimensions of glass-sealed ceramic quad flat package (G-QFP):

size and recommended range:

--- Part 6-9: General rules for drawing surface mount semiconductor device package outline drawings Plastic quad flat package (P-QFP)

Design Guidelines for Integrated Circuits: The purpose is to specify the standard outline drawing, dimensions of plastic quad flat package (P-QFP) integrated circuits

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(P-VSON) size: The purpose is to specify the standard outline drawing, dimension

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(FLGA) Design Guidelines: The purpose is to specify the standard outline drawing, dimensions and promotion of fine-pitch land array package (FLGA):

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--- Part 6-13: Close pitch ball array package (FBGA) and close pitch land array package (FLGA) top open fixture

design guidelines: The purpose is to specify the top of the fine pitch ball array package (FBGA) and the fine pitch land array package (FLGA)

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--- Part 6-14: General rules for drawing surface mount semiconductor device package outline drawings Small outline J-lead package (SOJ)

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--- Part 6-15: General rules for drawing surface mount semiconductor device package outline drawings Small outline package (SOP) Dimensional measurement

Quantitative method: The purpose is to specify the dimensional measurement method of Small Outline Package (SOP):

--- Part 6-16: Ball Array Package (BGA), Land Array Package (LGA), Fine Pitch Ball Array Package (FBGA) and dense

Glossary of pitch land array package (FLGA), semiconductor test and burn-in fixtures: The purpose is to specify the ball array package

(BGA), Land Array Package (LGA), Fine Pitch Ball Array Package (FBGA) and Fine Pitch Land Array Package

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--- Part 6-17: Stacked Package Design Guidelines for Fine Pitch Ball Array Package (FBGA) and Fine Pitch Land Array Package (FL-

GA): The purpose is to specify the standard outline of the fine-pitch ball array package